

Project Name :NTSN1521

Platform : Haswell + Lynx Point+N16P-GX

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26. HDD/ODD /MINI CARD

27. LAN RTL8411-CG/CARD READER/15DB

28. CODEC(ALC269Q)/INT MIC/SPKR

29. EXT_MIC/C_PAD/USB/FAN/G-SEN

30. DC IN/TPM/M-sata/D-Resis

31. CPU CORE (OZOZ8127)

32. +1.05V(NB671)/+0.75VS/+1.5V

33. +1.5VS/+5VA (OZ8153)

34. BATT IN/CHARGER(OZ8660)

35. TP/LED/WEBCAM/USB

36. VCC SW/+3.3VA/HIGH-SPEED CAP

37. INTEL LAN(82579LM)

38. Reserved

39. History

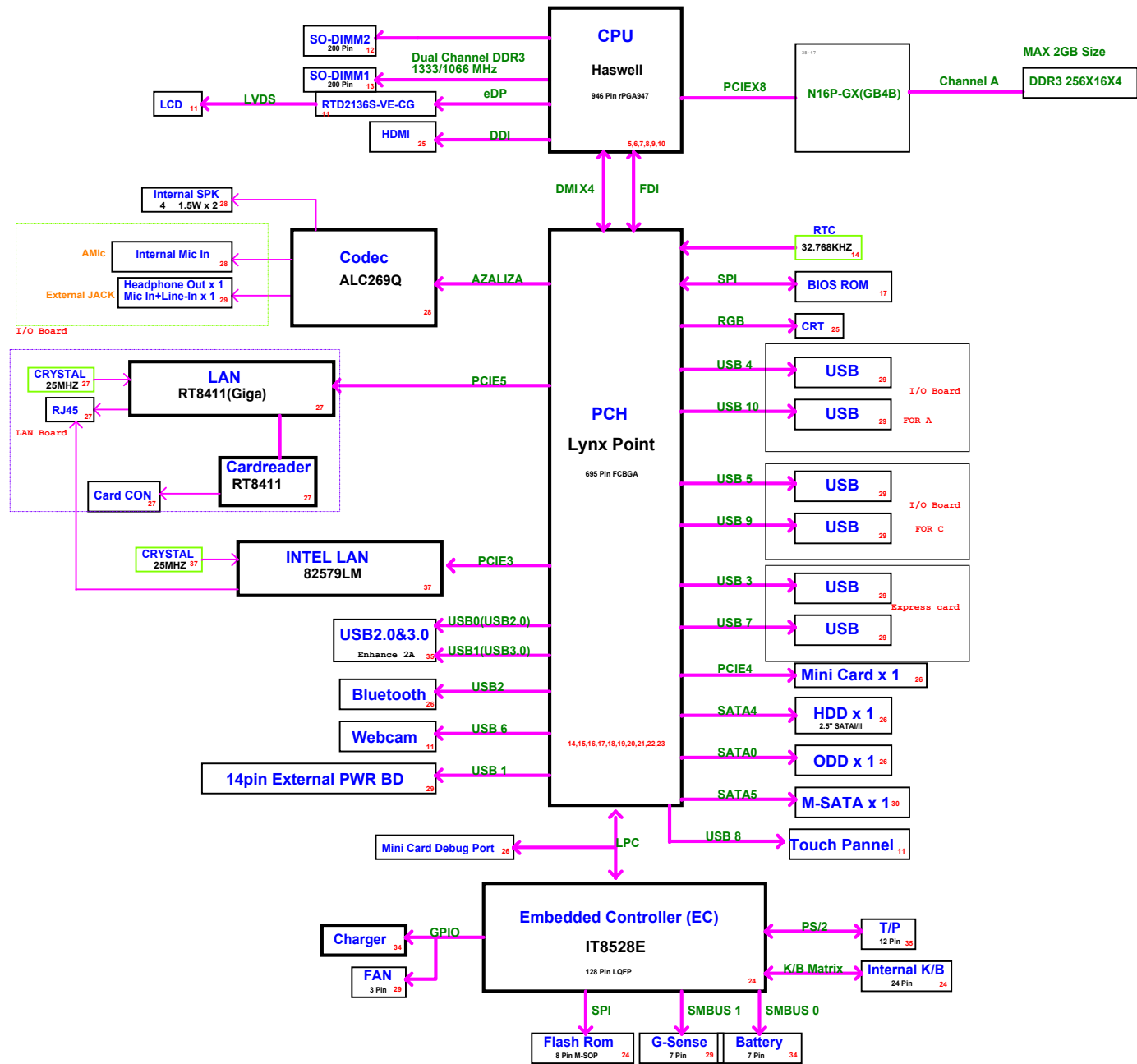
M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

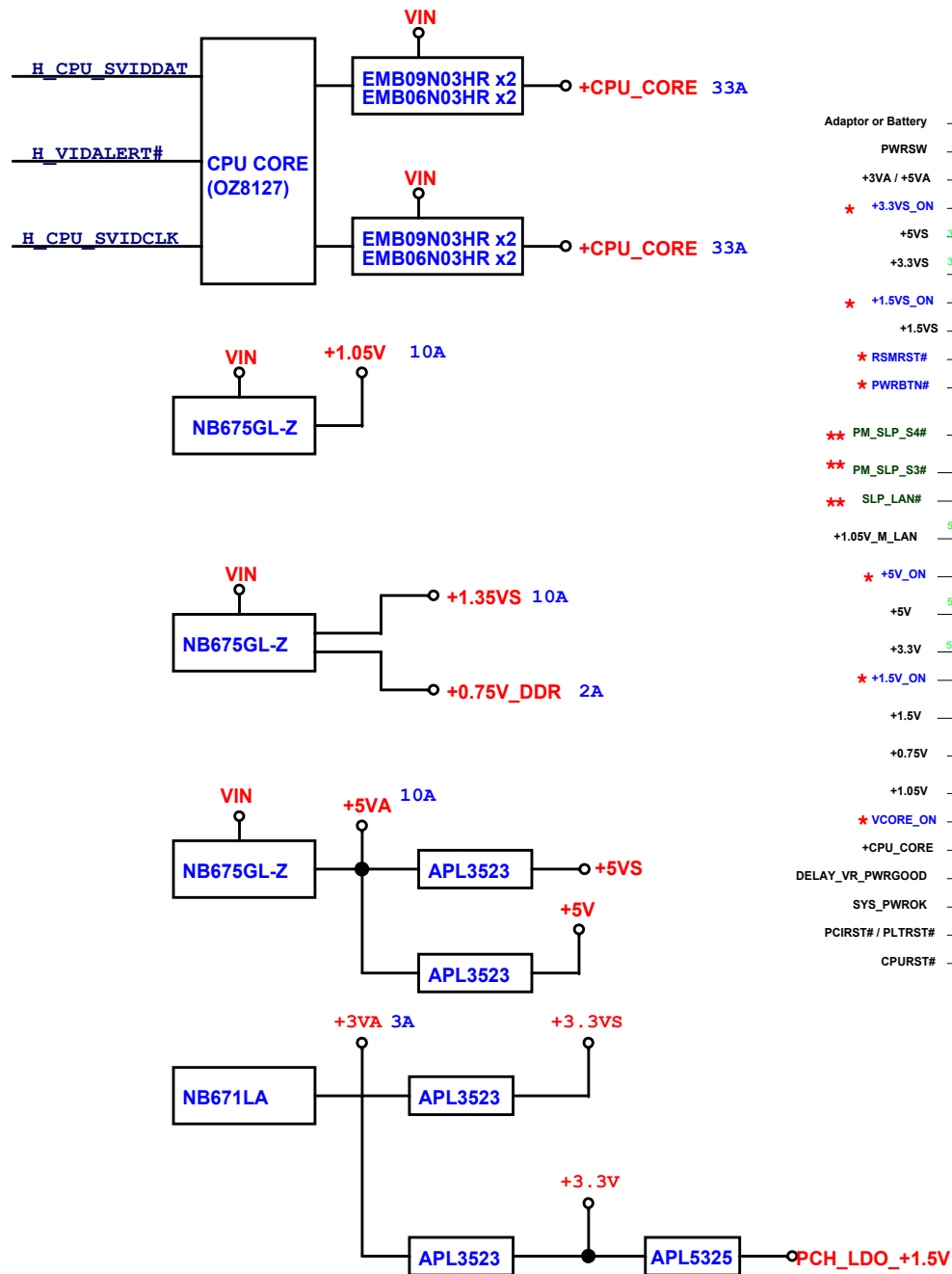
Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

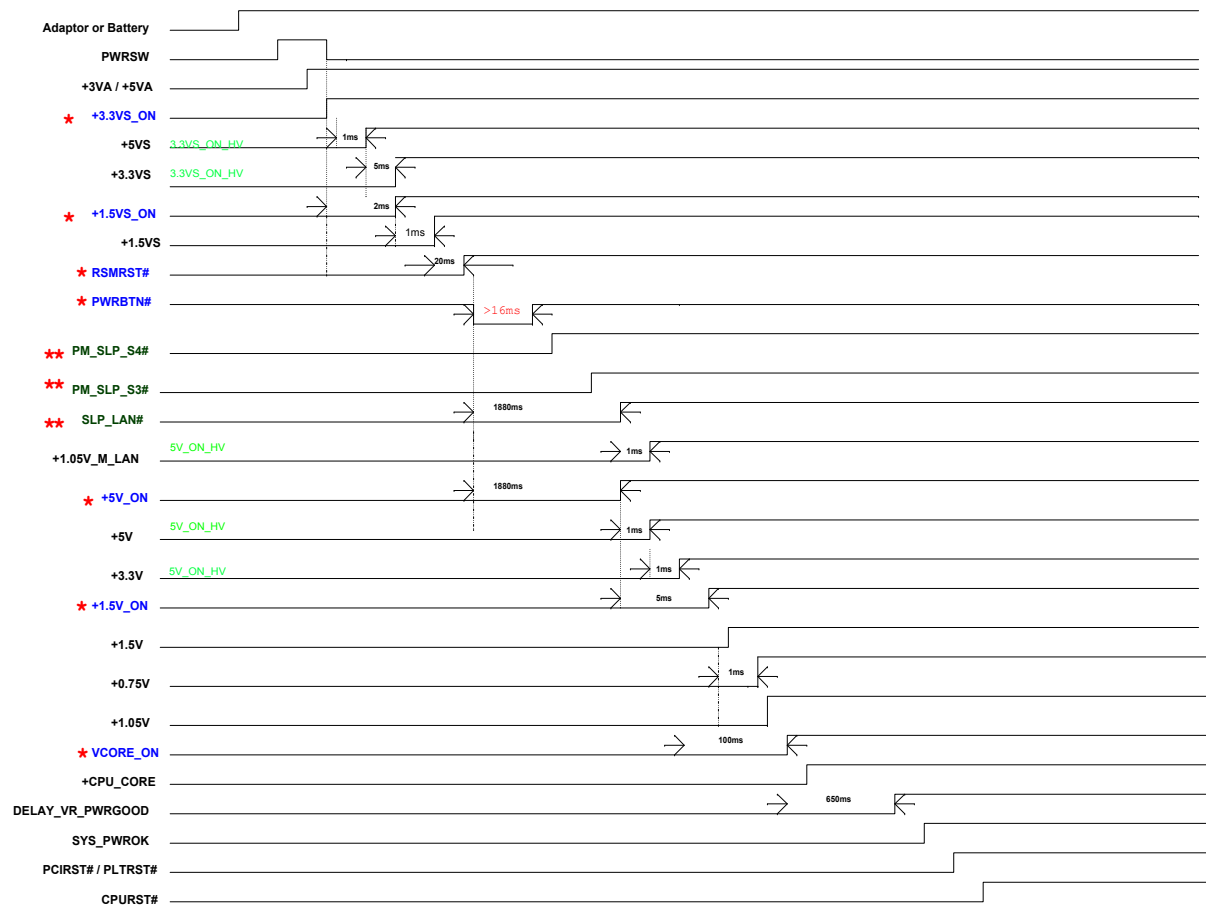
SYSTEM BLOCK DIAGRAM



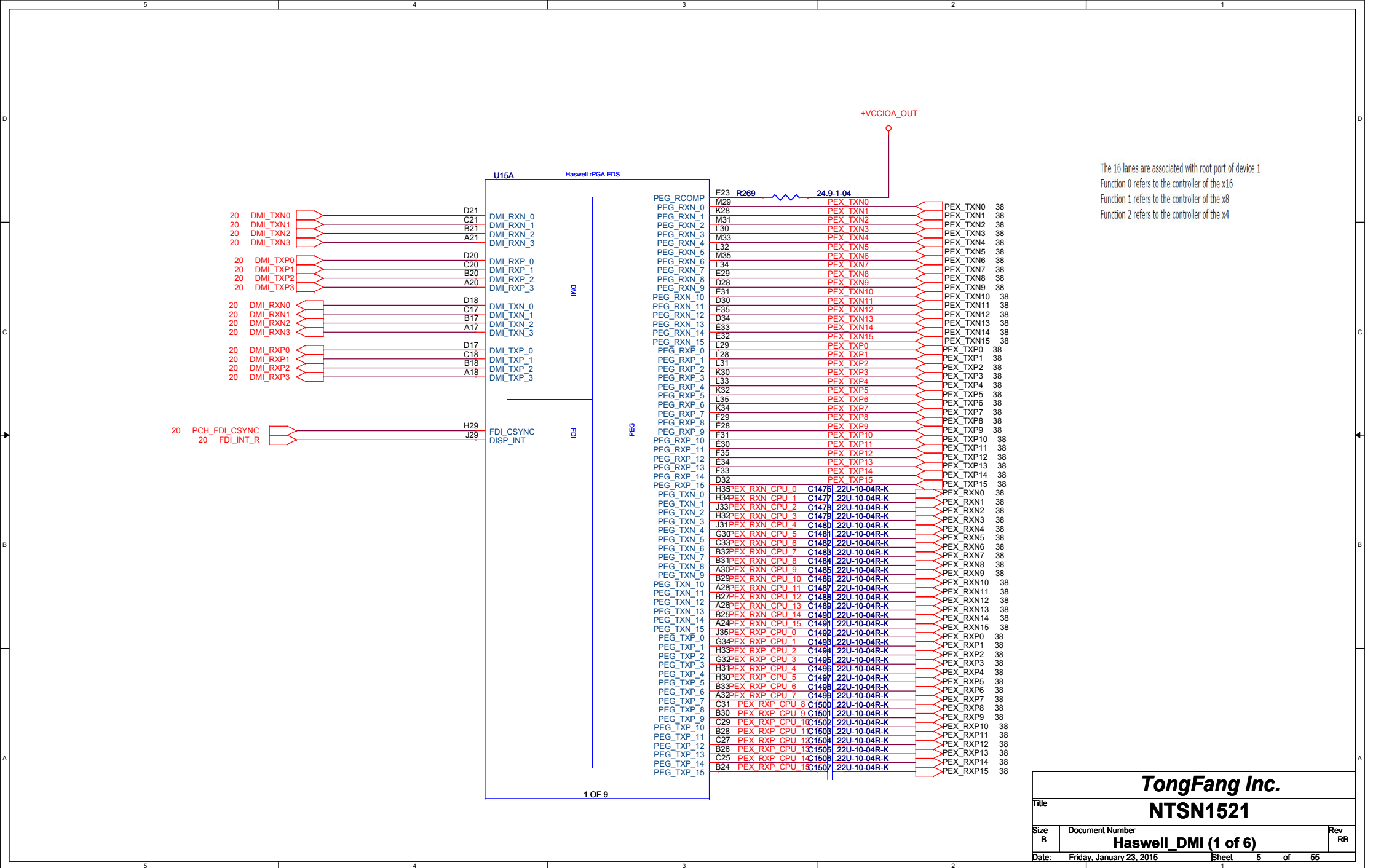
POWER BLOCK DIAGRAM



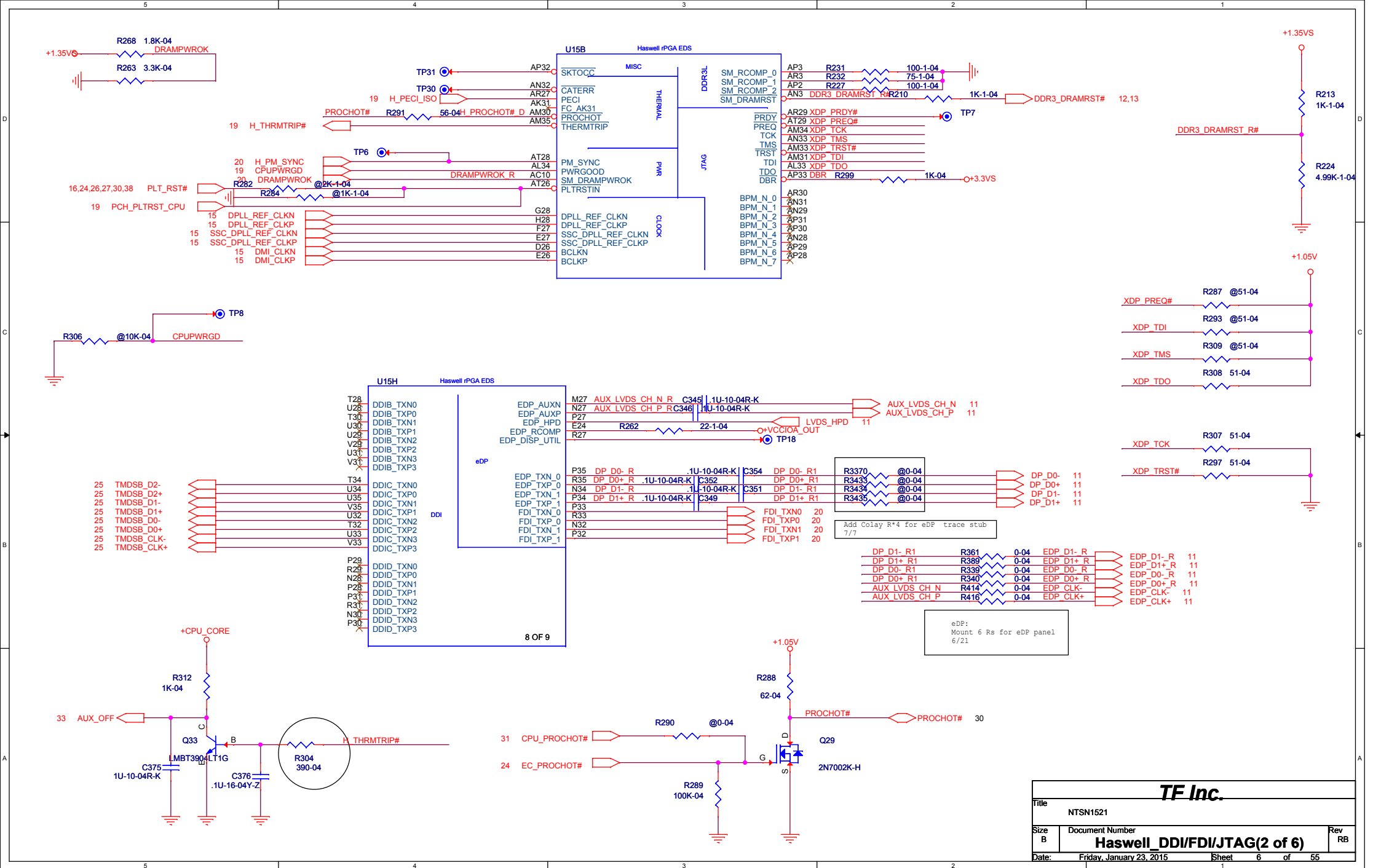
System Poewr On Sequence

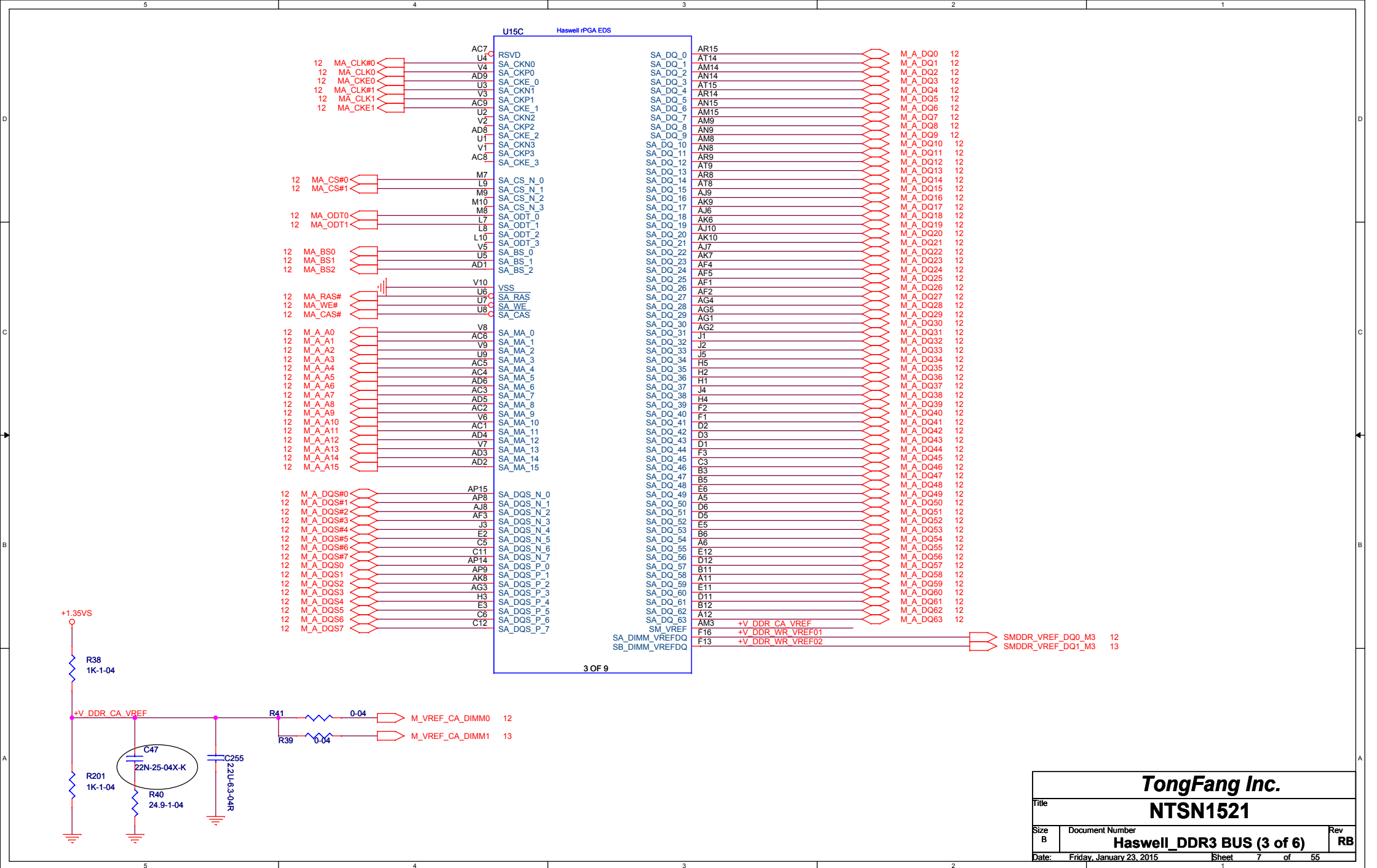


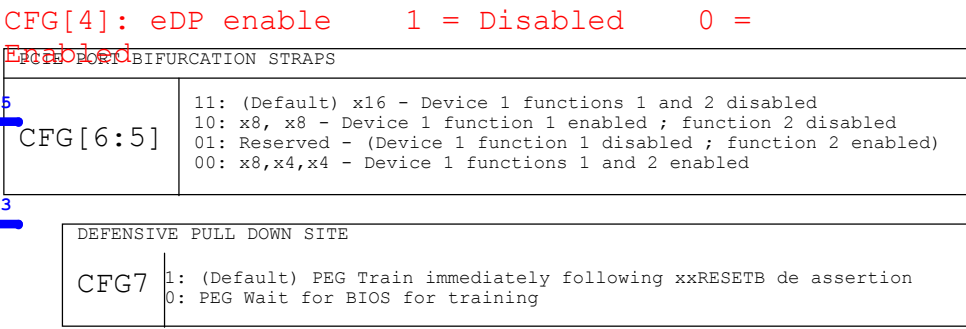
★ EC Control Pin (O/P)
★★ EC Control Pin (I/P)



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NTSN1521		
Size B	Document Number	Rev RB
Haswell_DMI (1 of 6)		
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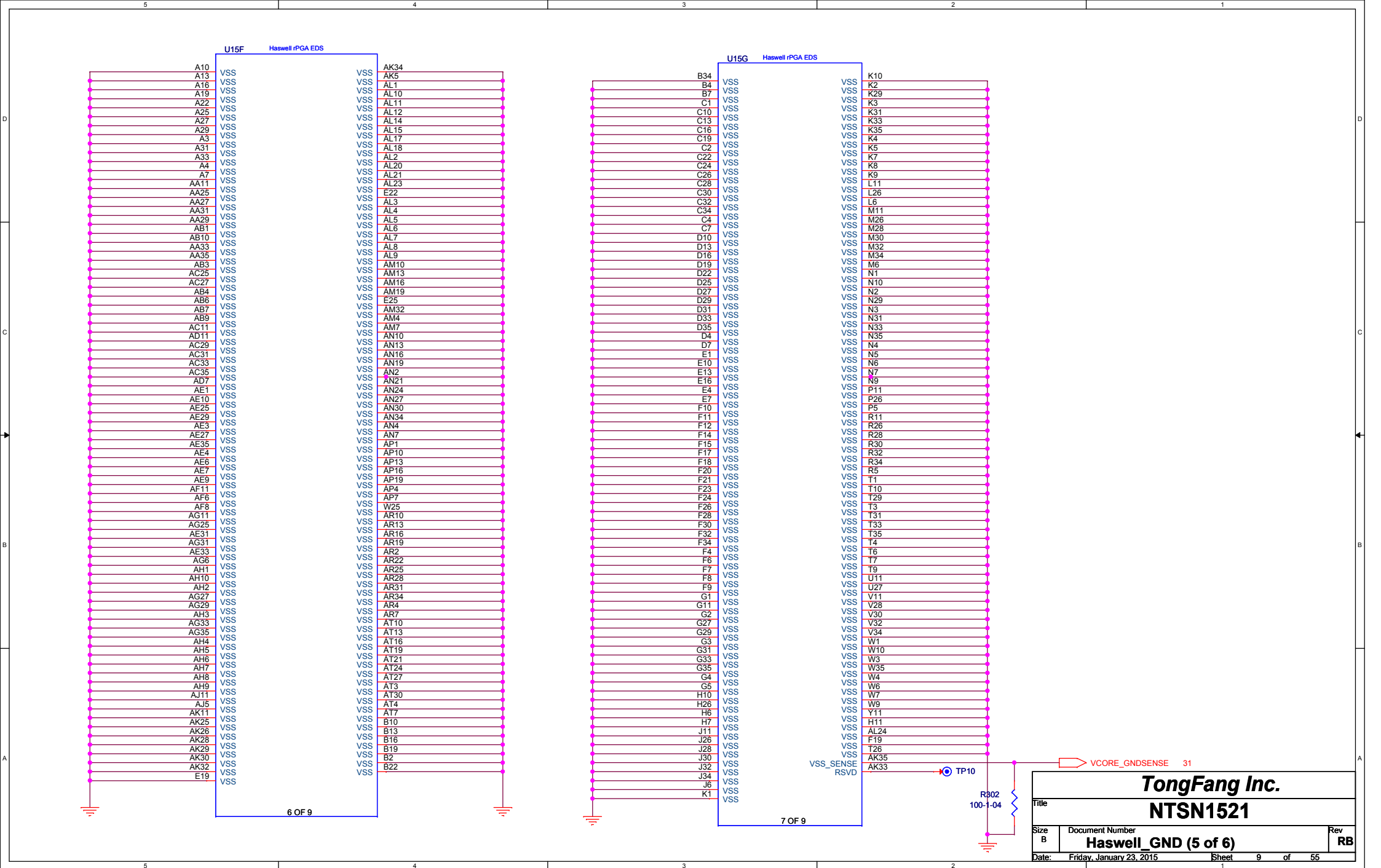


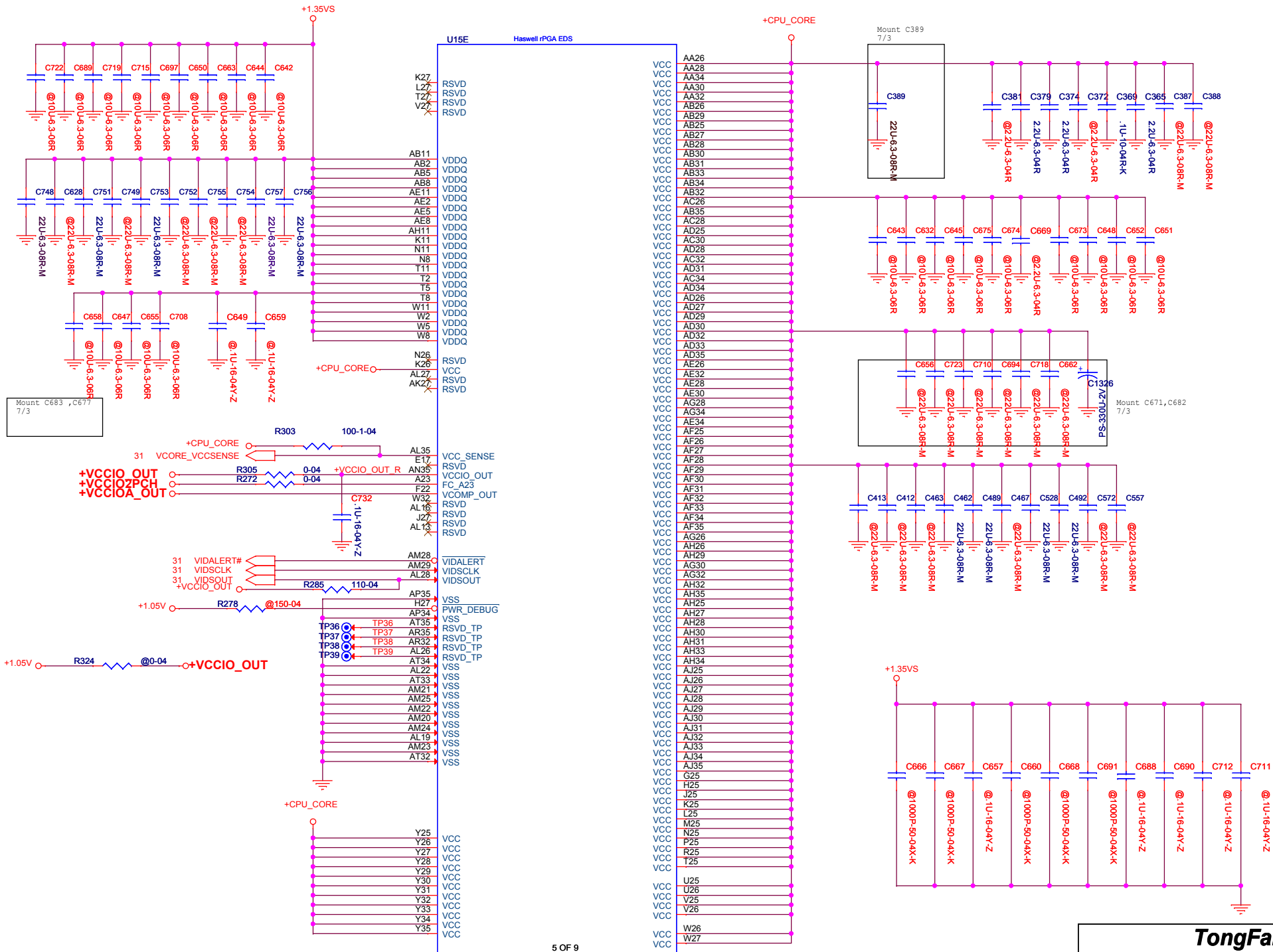


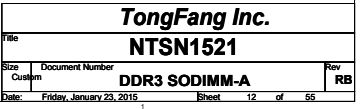
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1: (DEFAULT) NORMAL OPERATION;
   LANE# DEFINITION MATCHES
   SOCKET PIN MAP DEFINITION
0: LANE REVERSAL

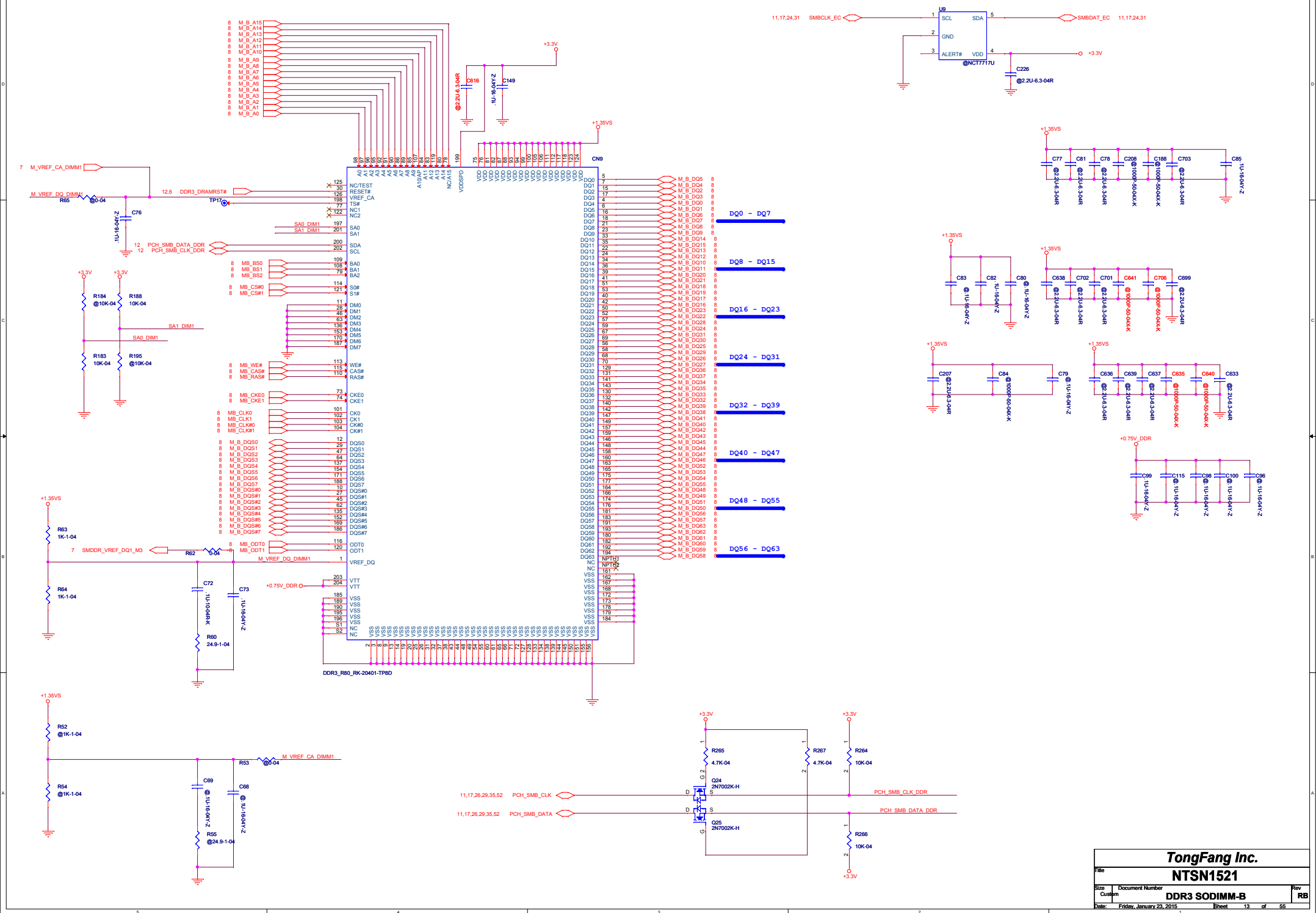
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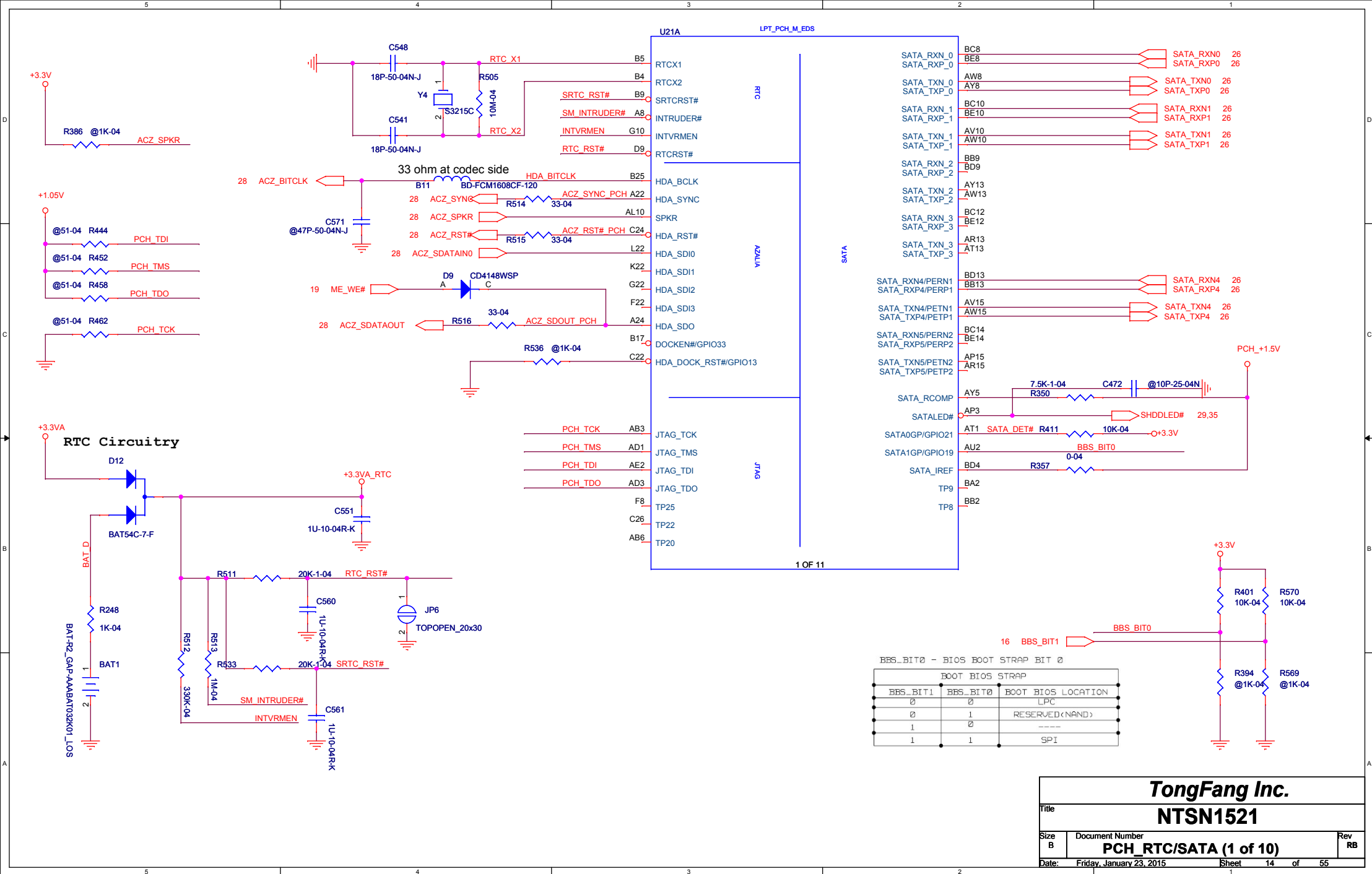



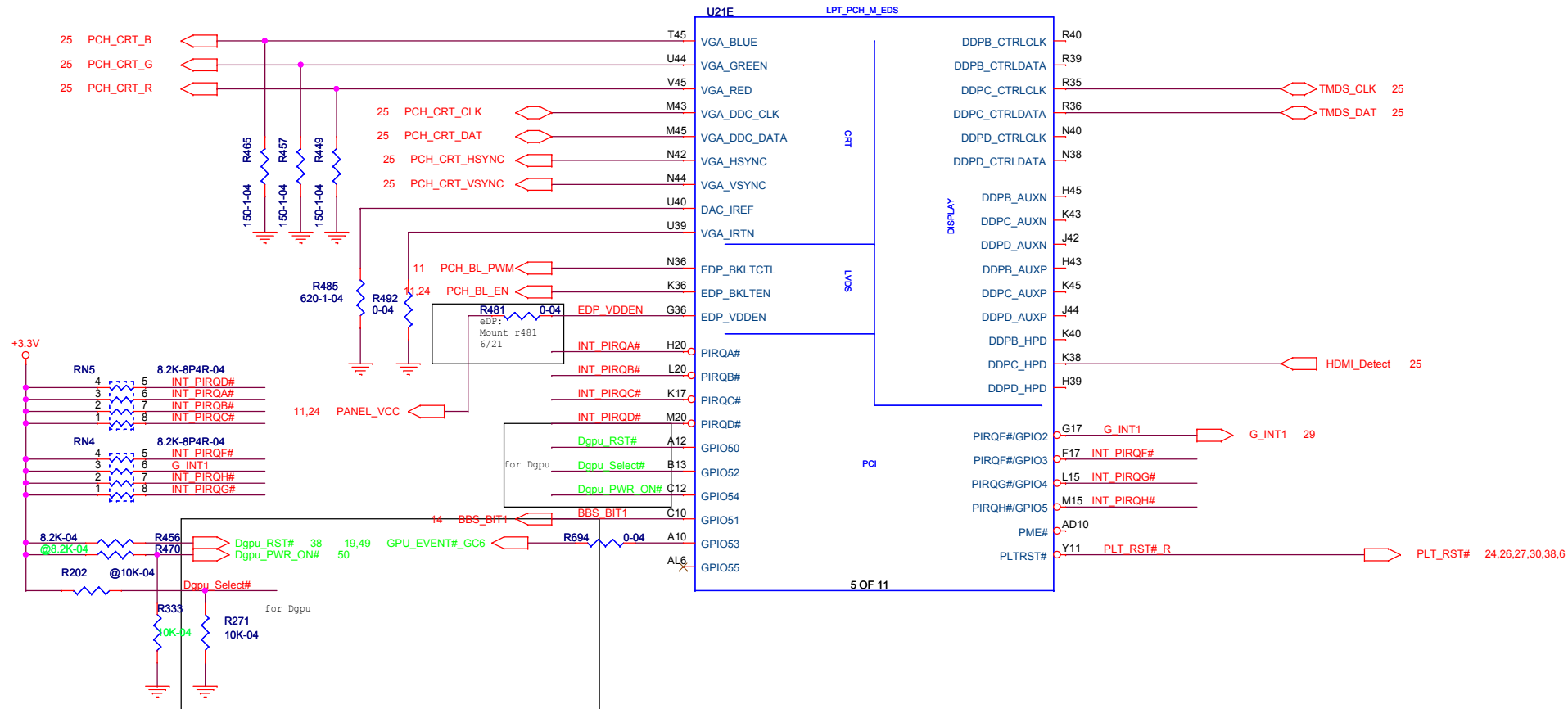




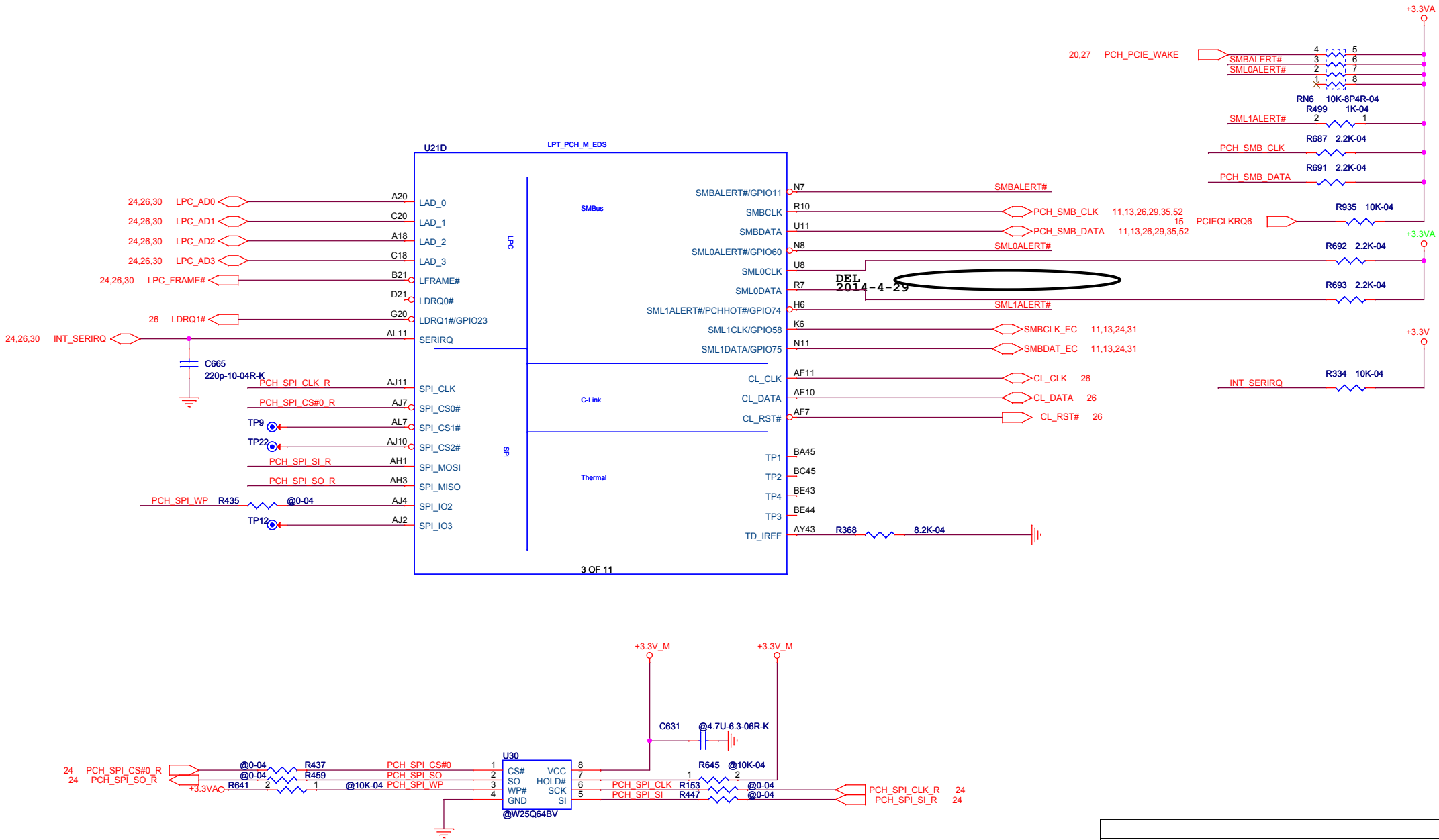
CPU Thermal Sensor



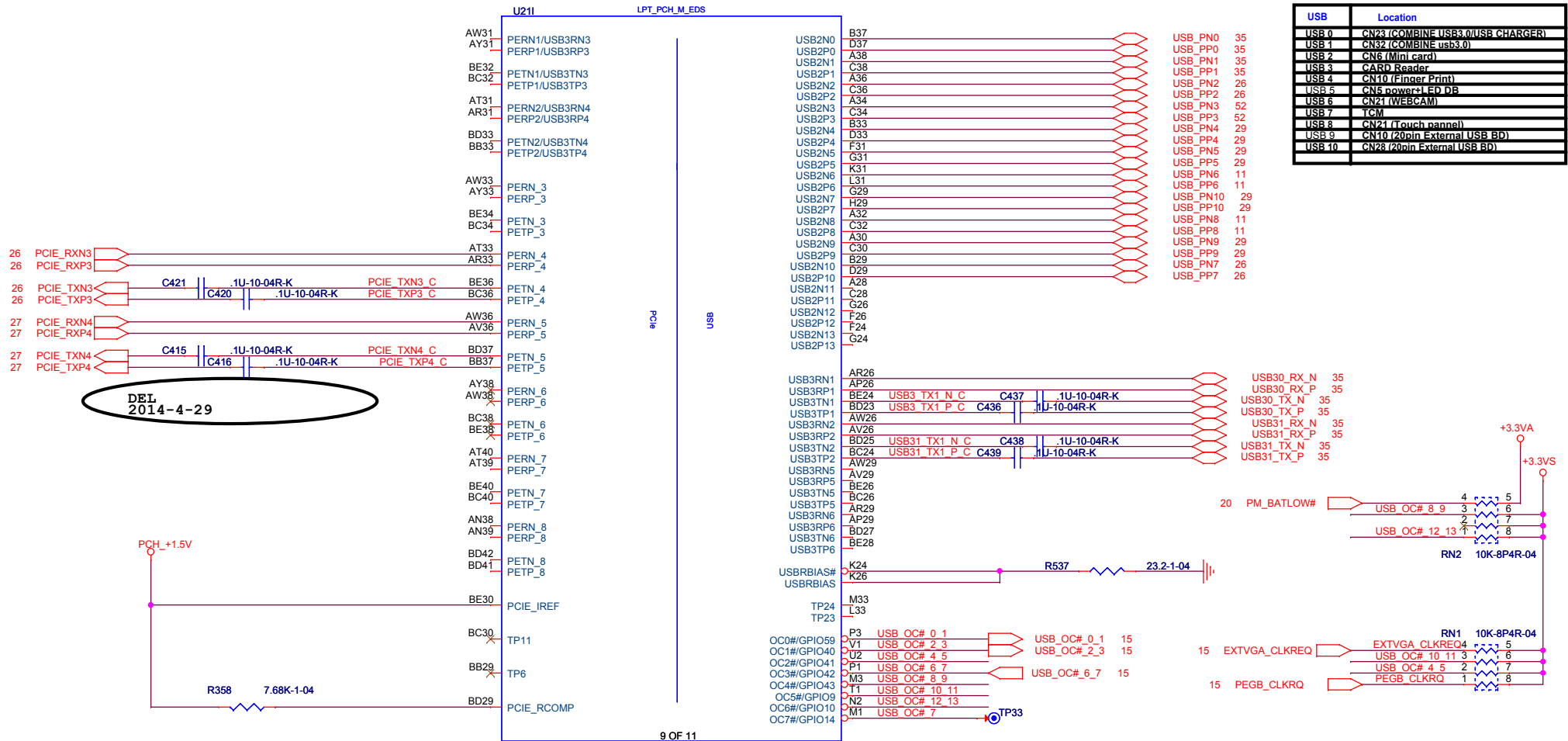


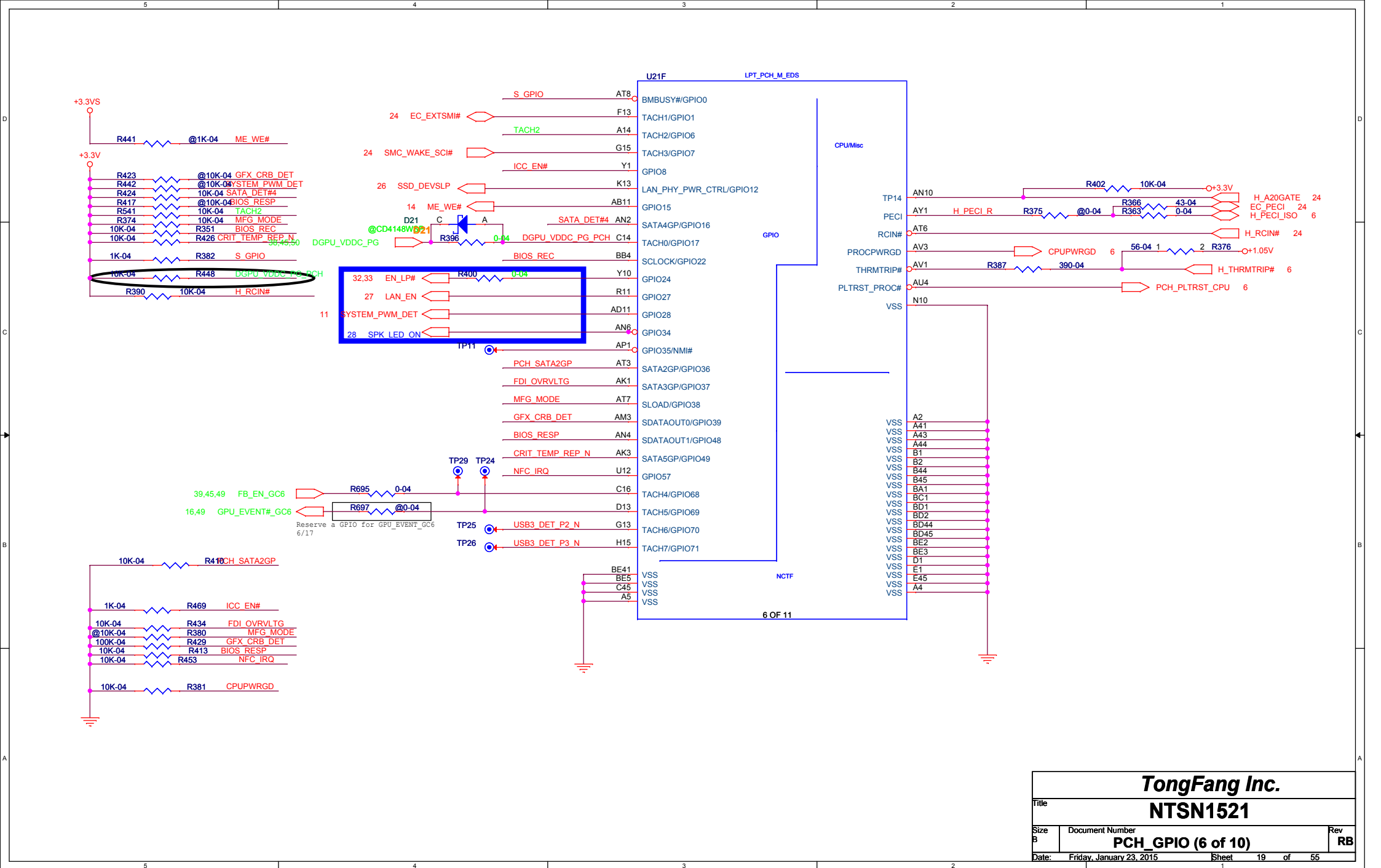


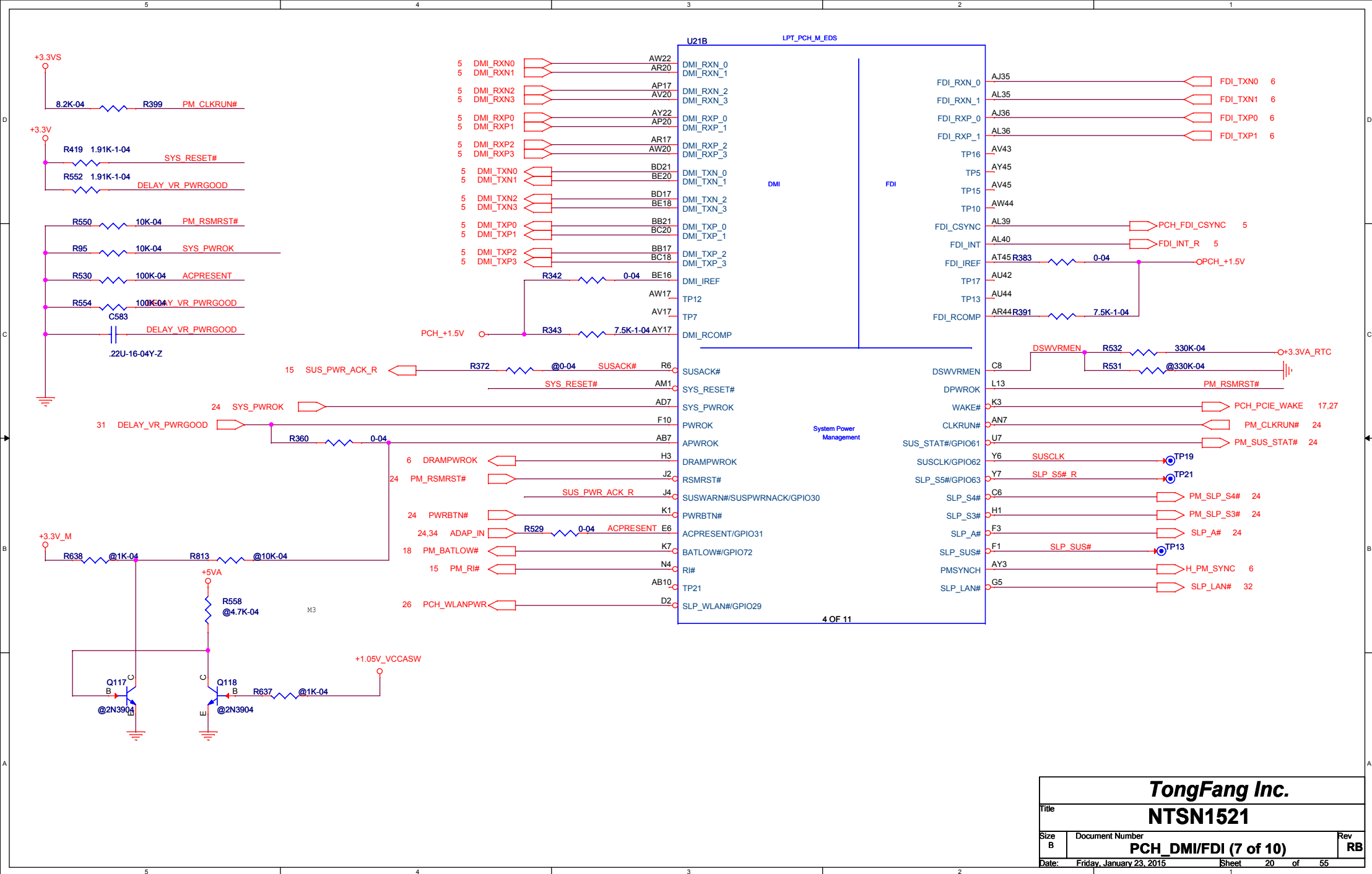
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Title			
NTSN1521			
Size	Document Number	Rev	
B	PCH_PCH_VGA/LVDS (3 of 10)	RB	
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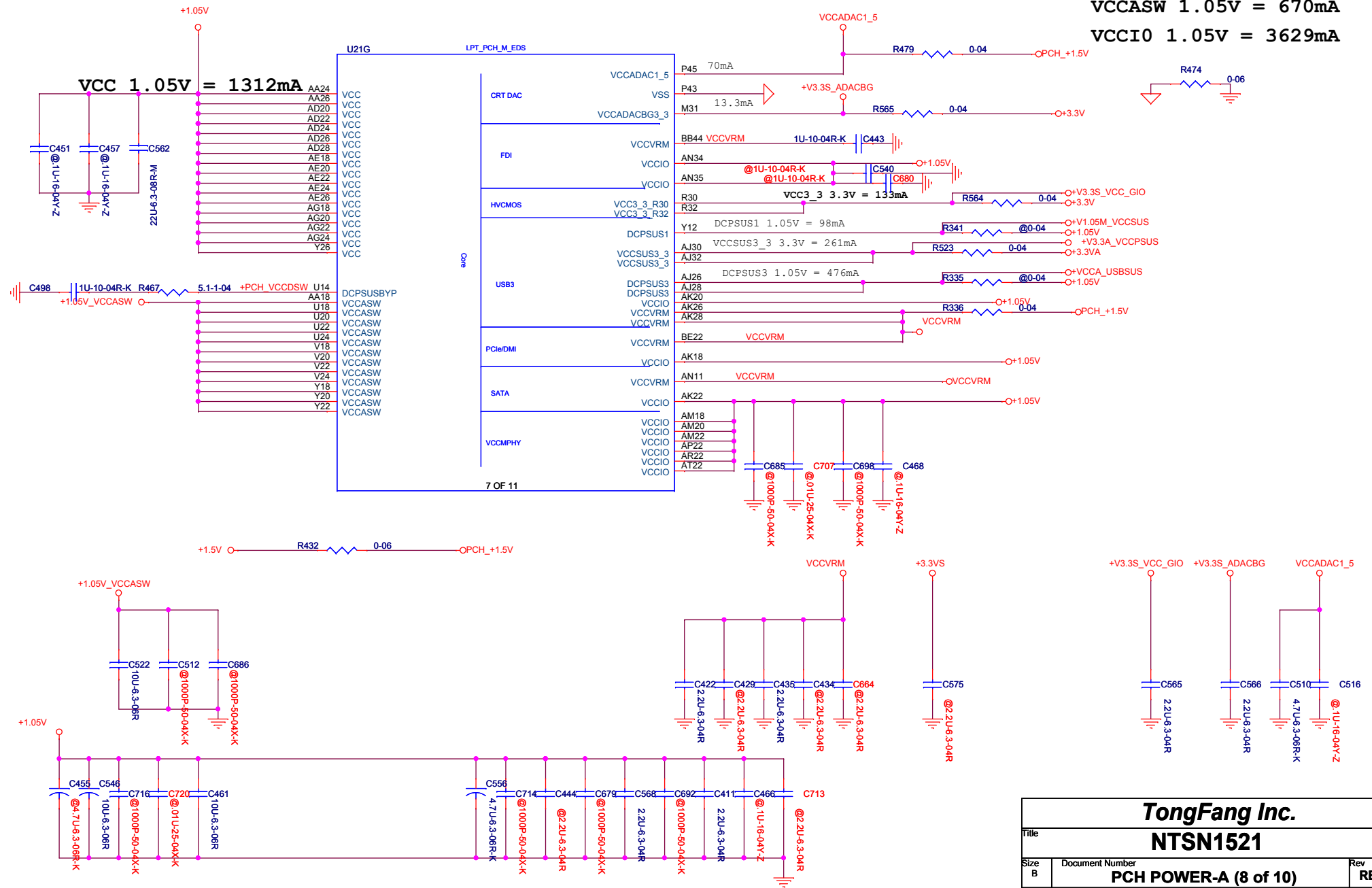
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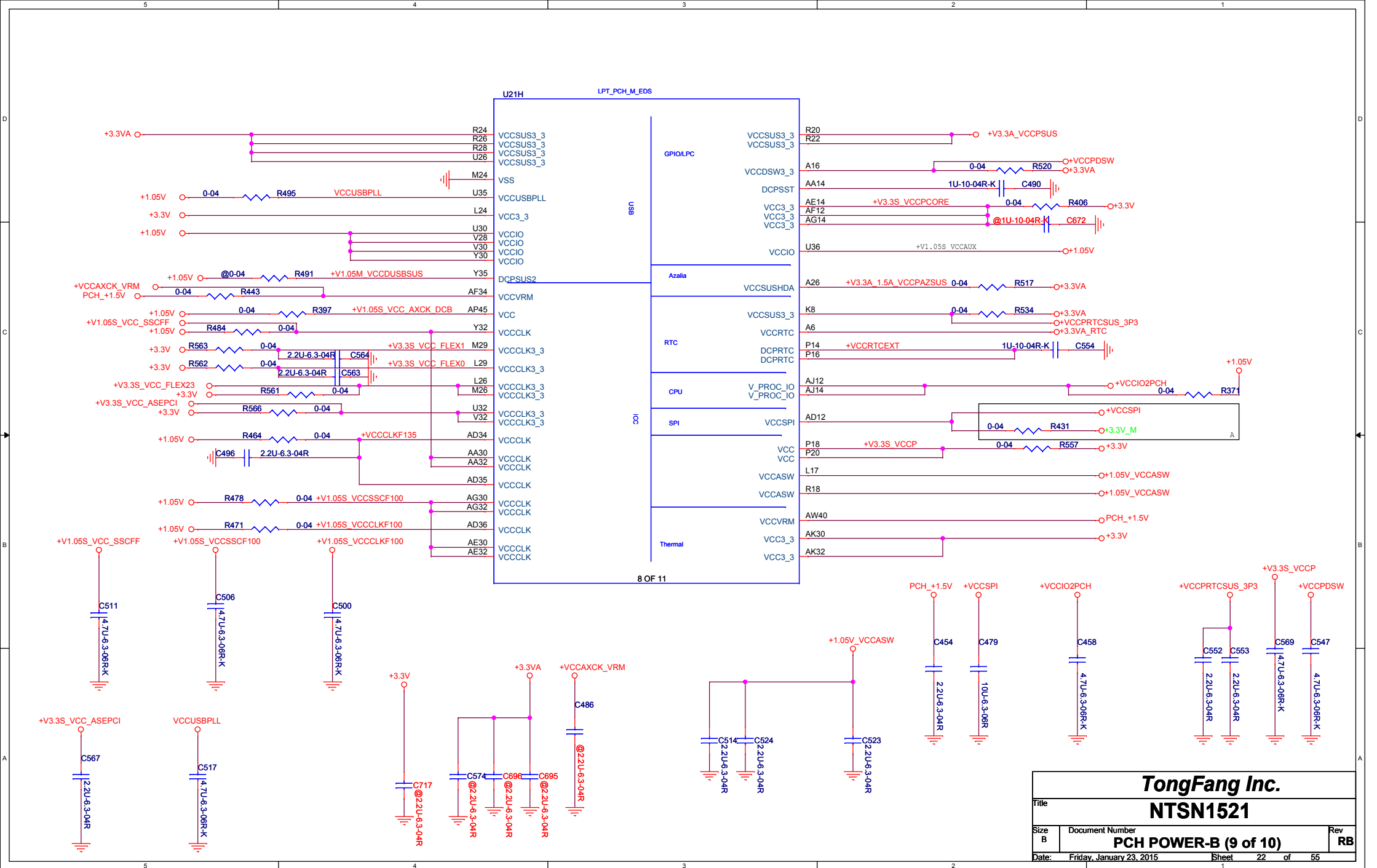


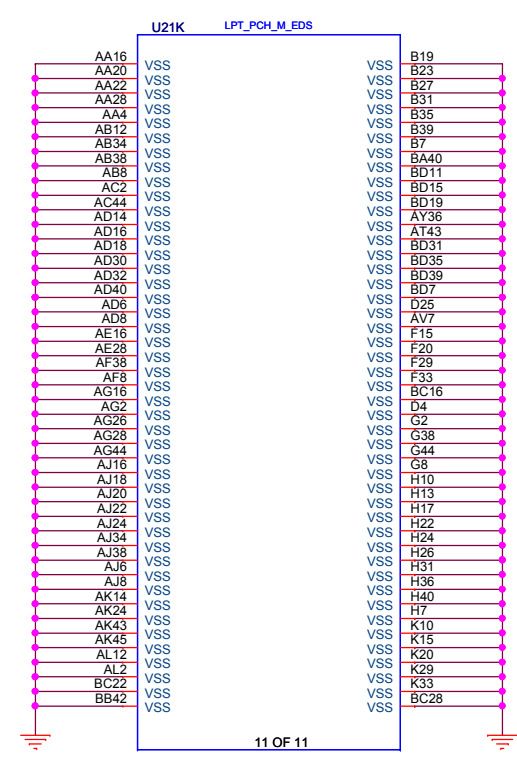
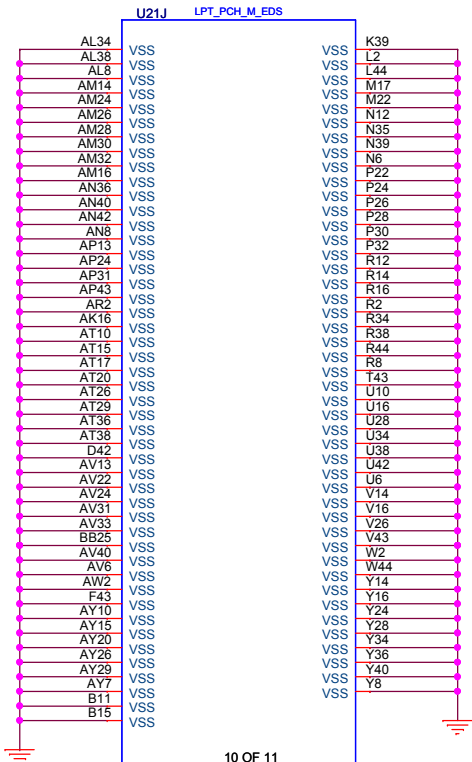


VCCI0 1.05V = 3629mA

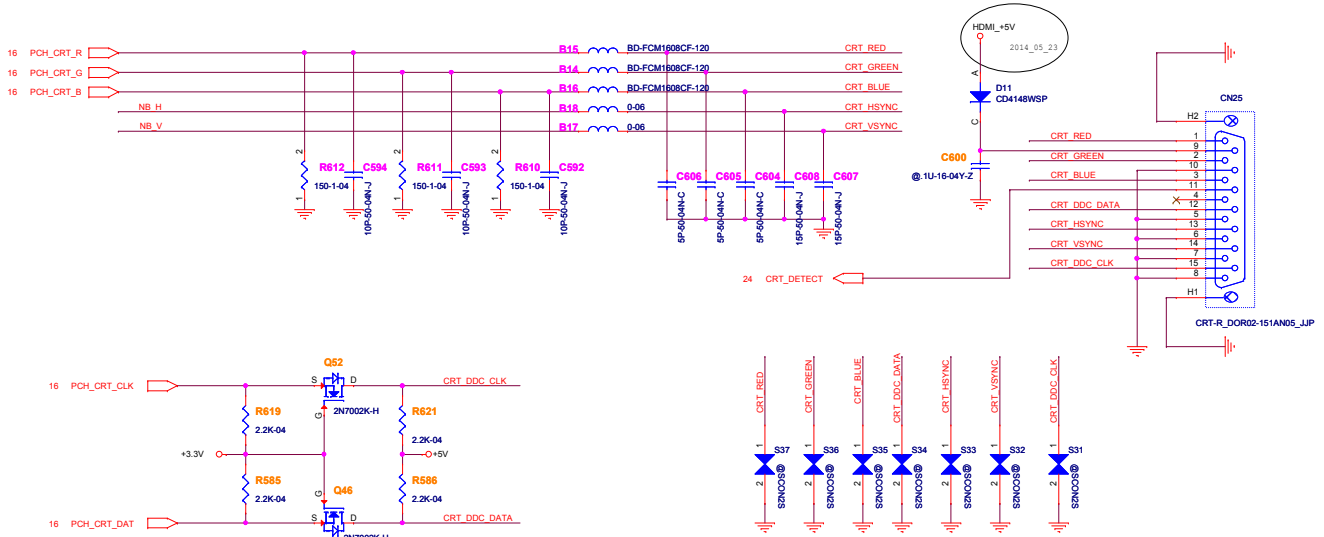
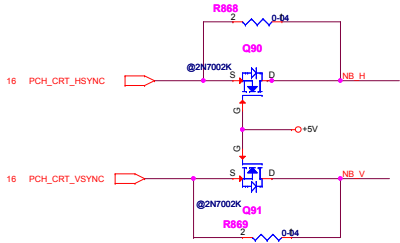


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	PCH POWER-A (8 of 10)					RB	
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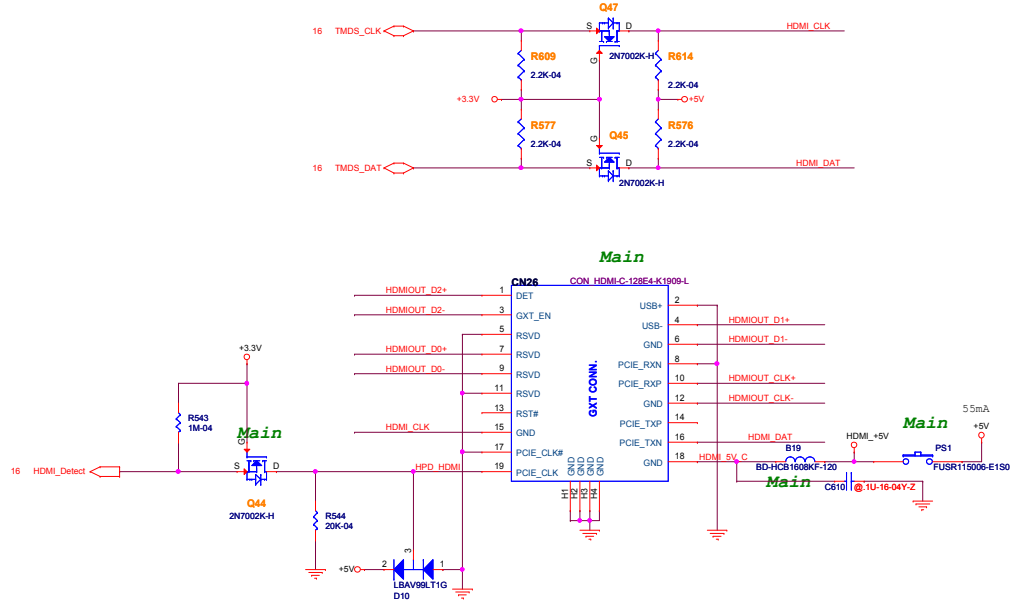
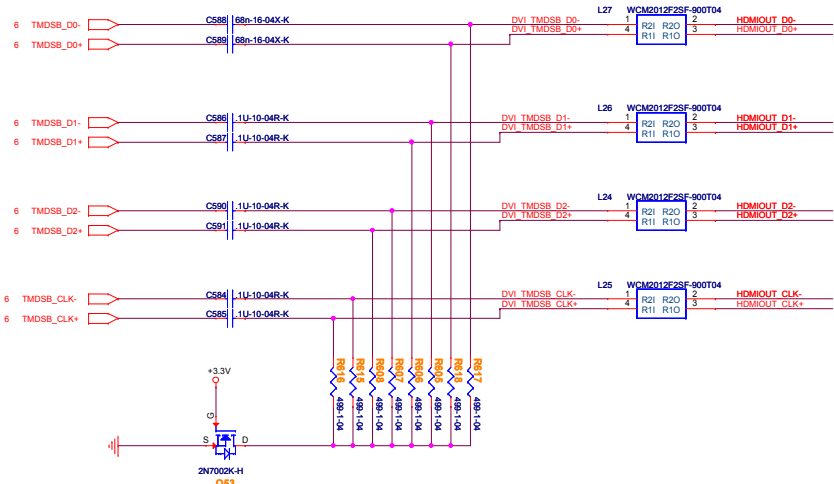




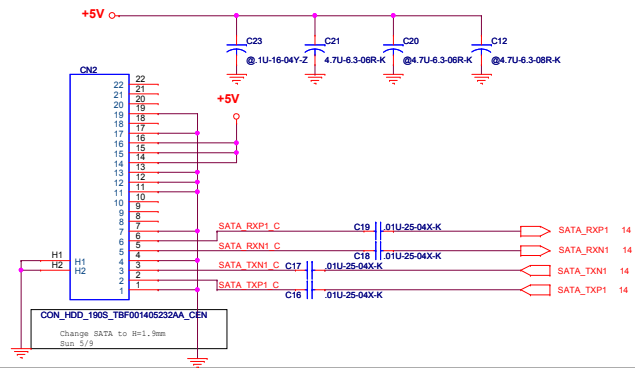
CRT CONN



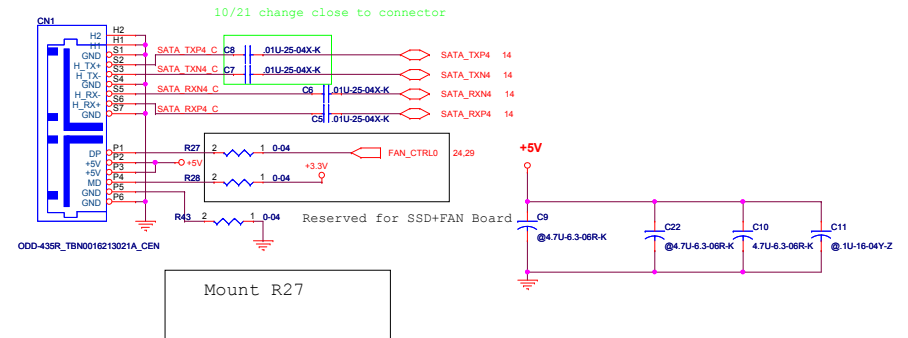
HDMI CONN



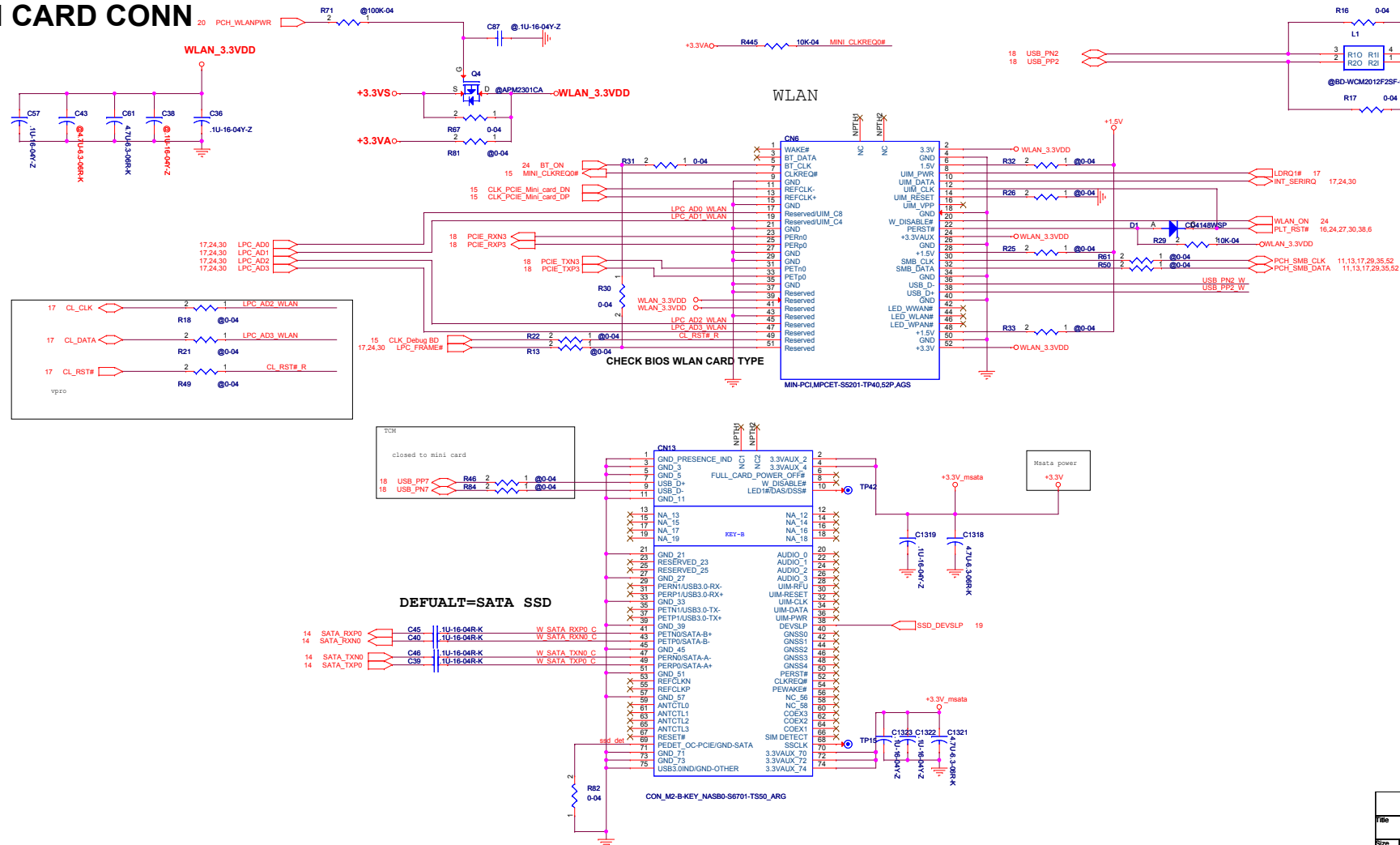
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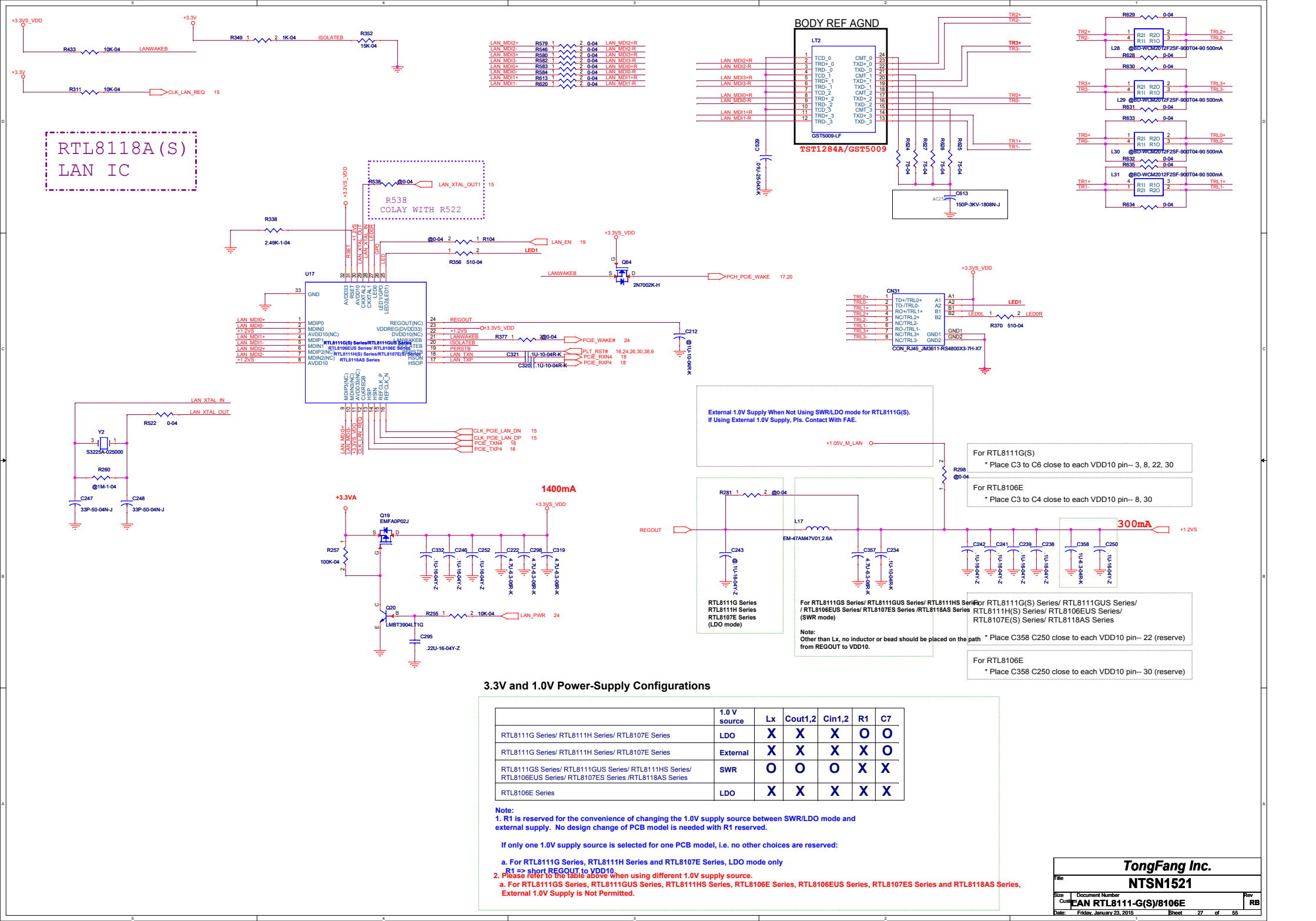


CD-ROM



MINI CARD CONN

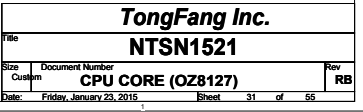




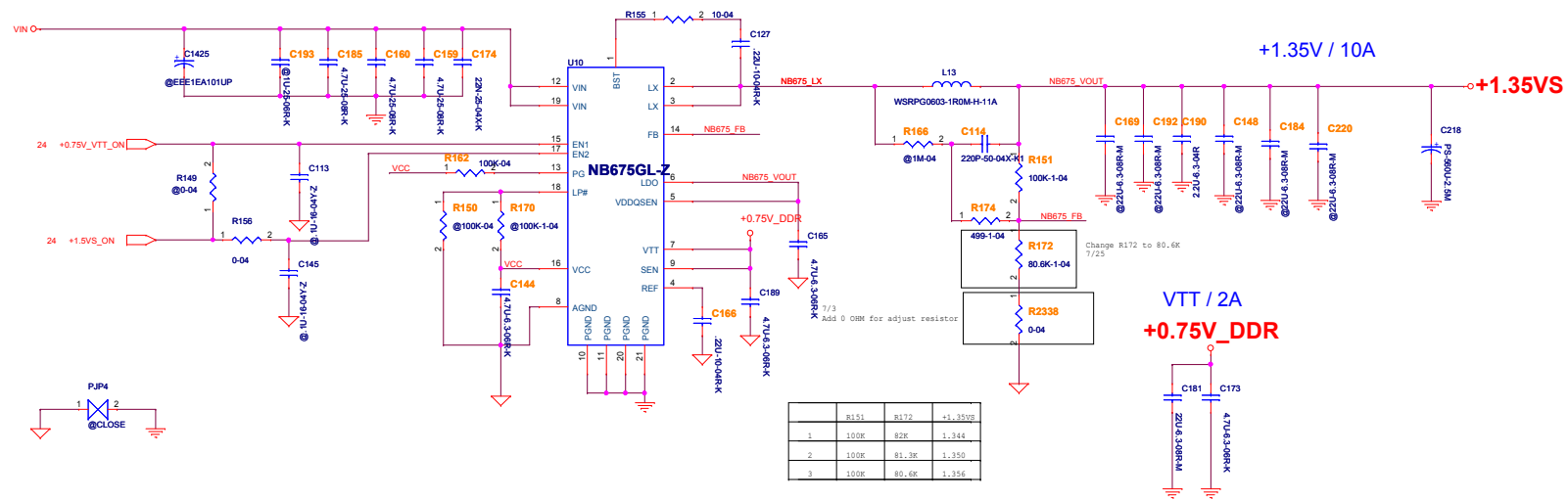
AMP VDD



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Size	Custom	Document Number	CODEC(ALC269)/INT MIC/SPKR				Rev
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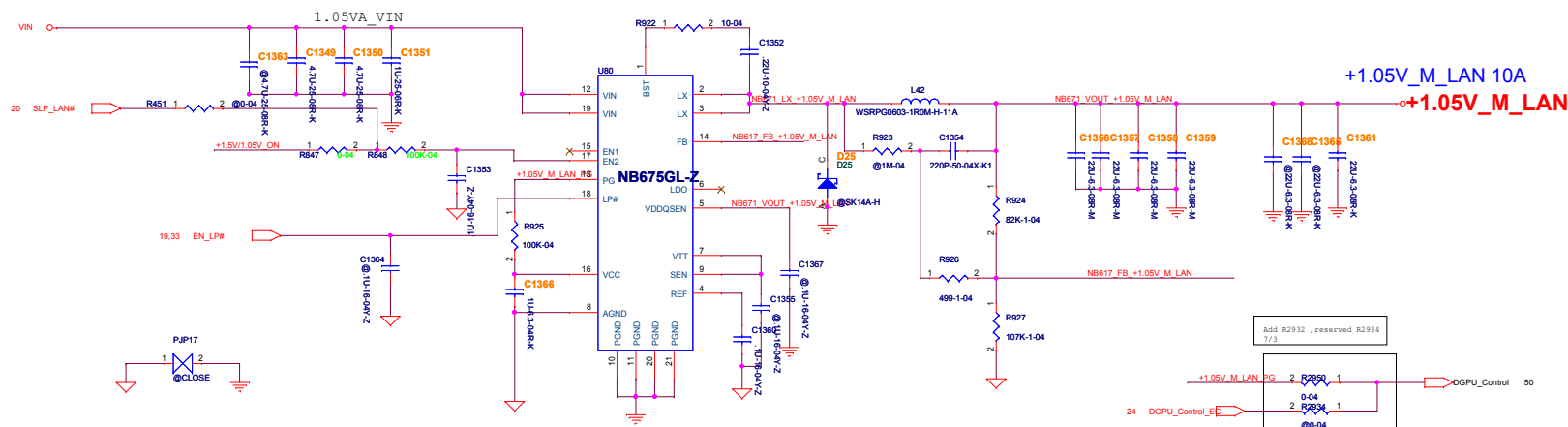
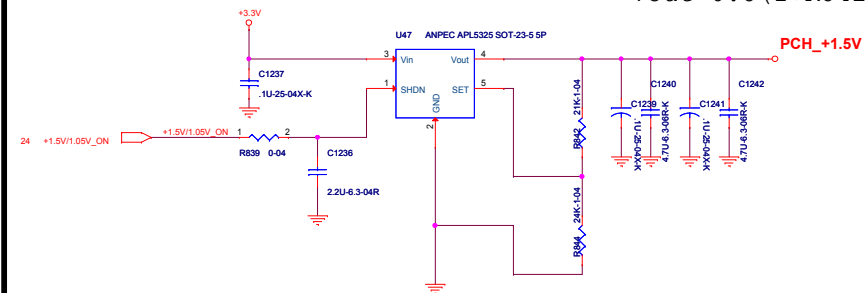


1.35VS/VTT Converter

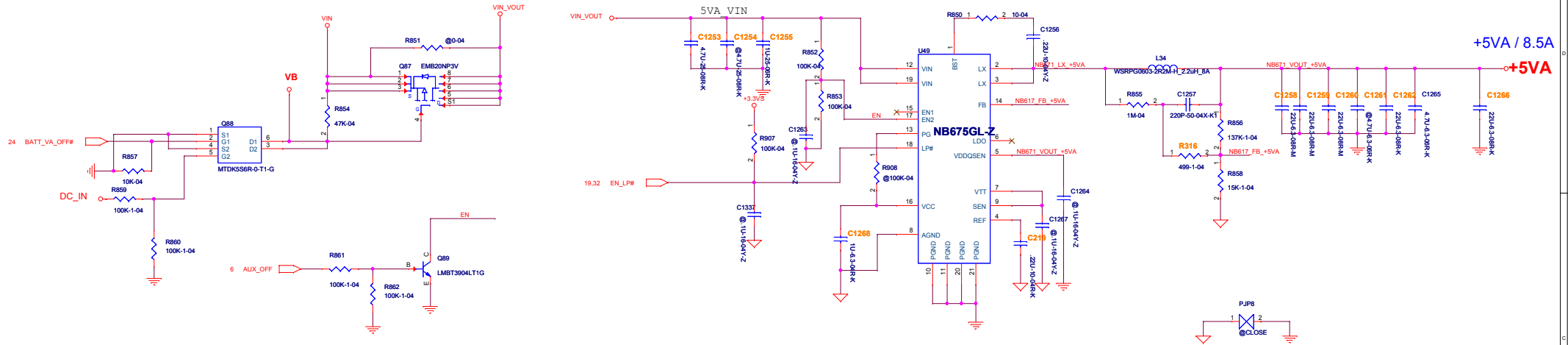


PCH_LDO_+1.5V

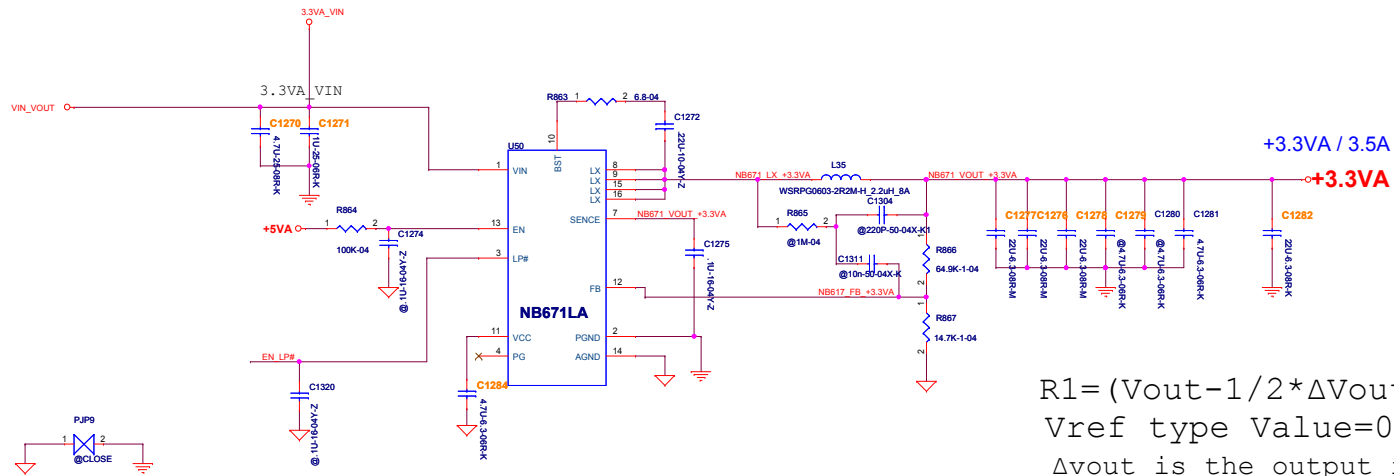
$$V_{out} = 0.8 (1 + R_{842}/R_{844})$$



5VA Converter



3.3VA Converter

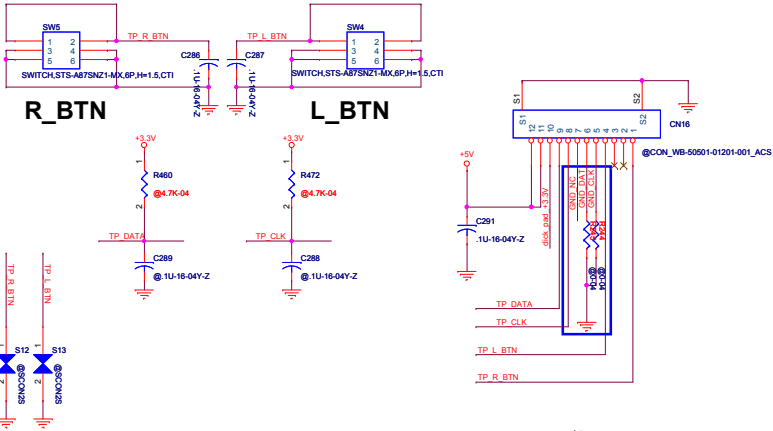


$$R1 = (V_{out} - 1/2 \cdot \Delta V_{out} - V_{ref}) / V_{ref} \cdot R2$$

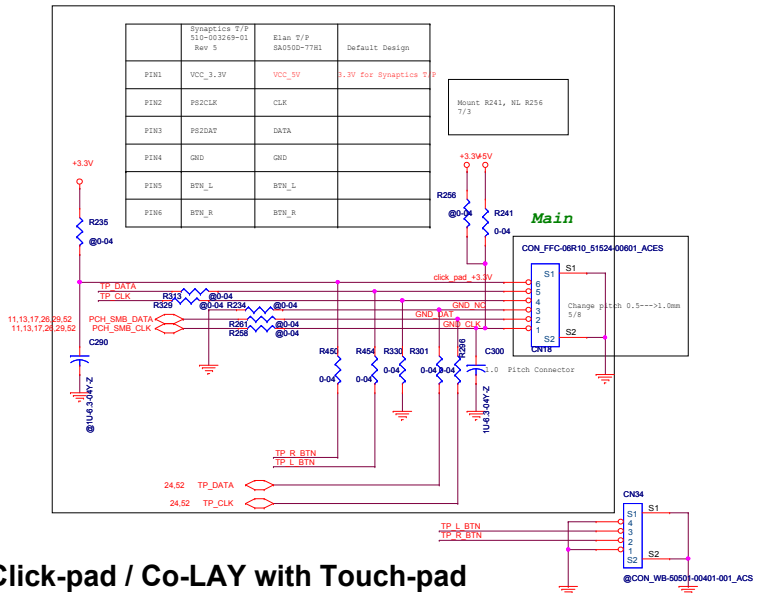
$$V_{ref} \text{ type Value} = 0.604 \text{ V}$$

$$\Delta V_{out} \text{ is the output ripple : } 5\% \cdot V_{out}$$

Touch Pad

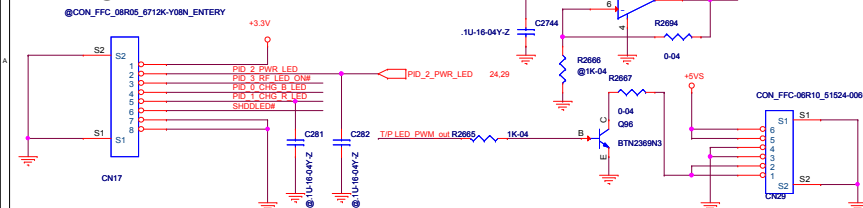


5/8

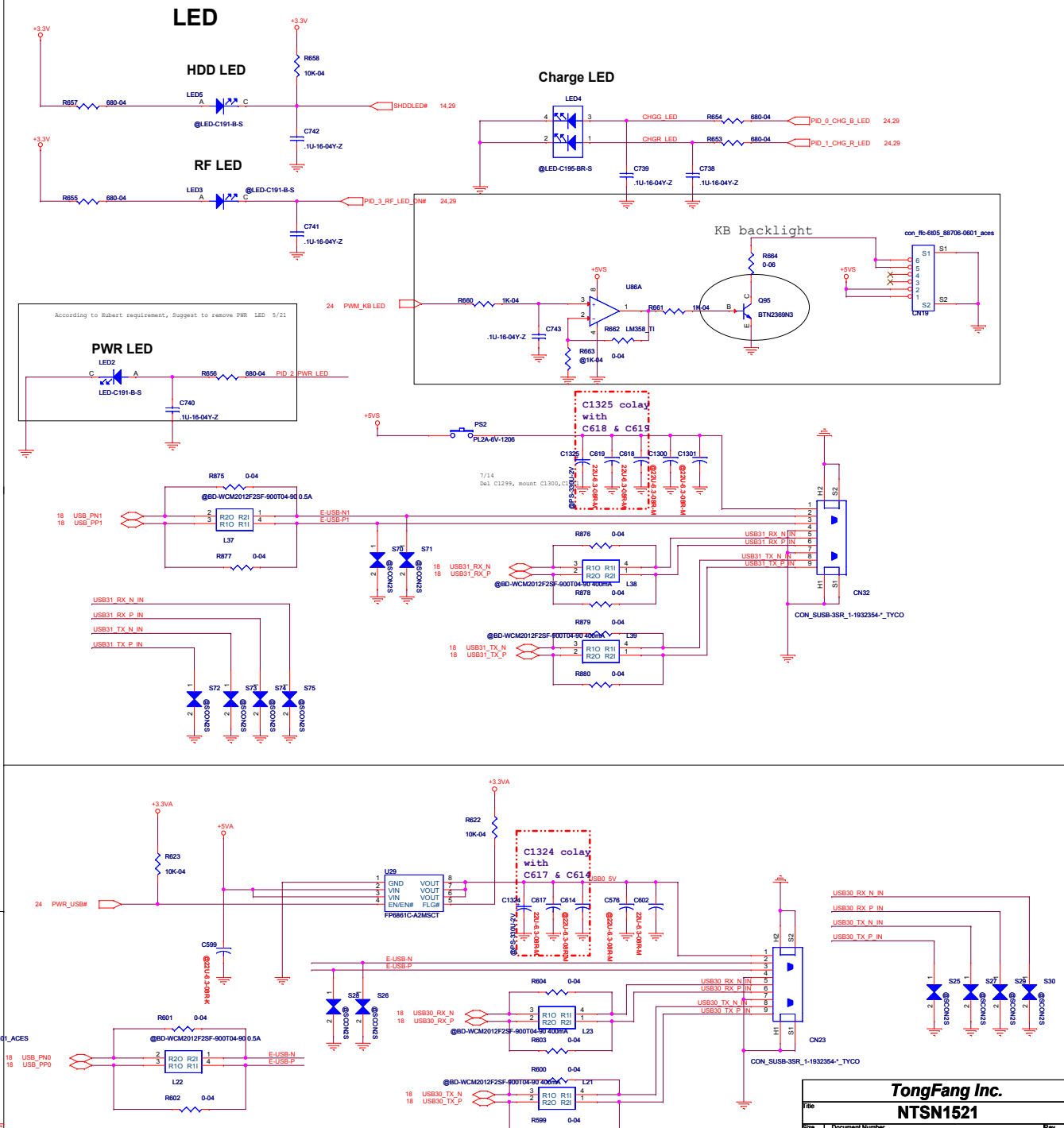


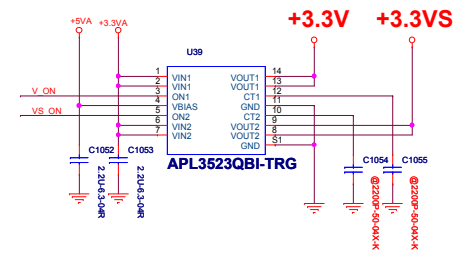
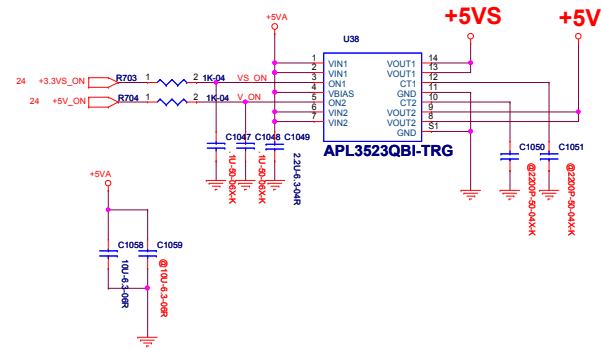
Click-pad / Co-LAY with Touch-pad

LED CONN

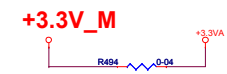
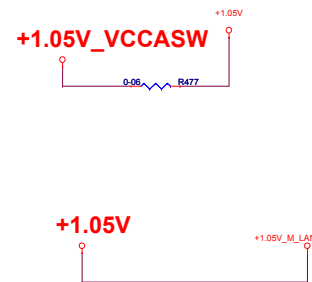
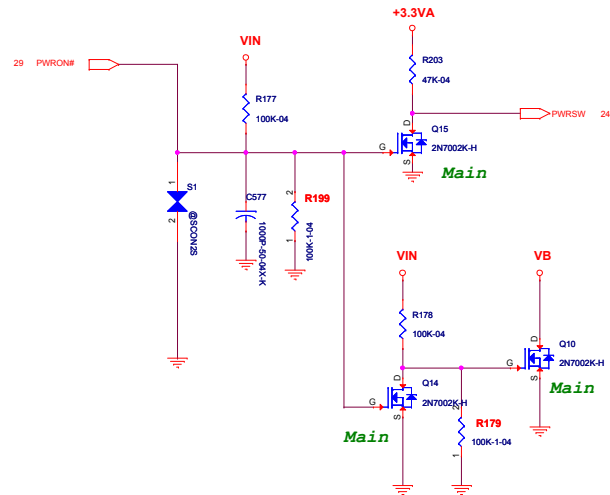


LED





PWR SW



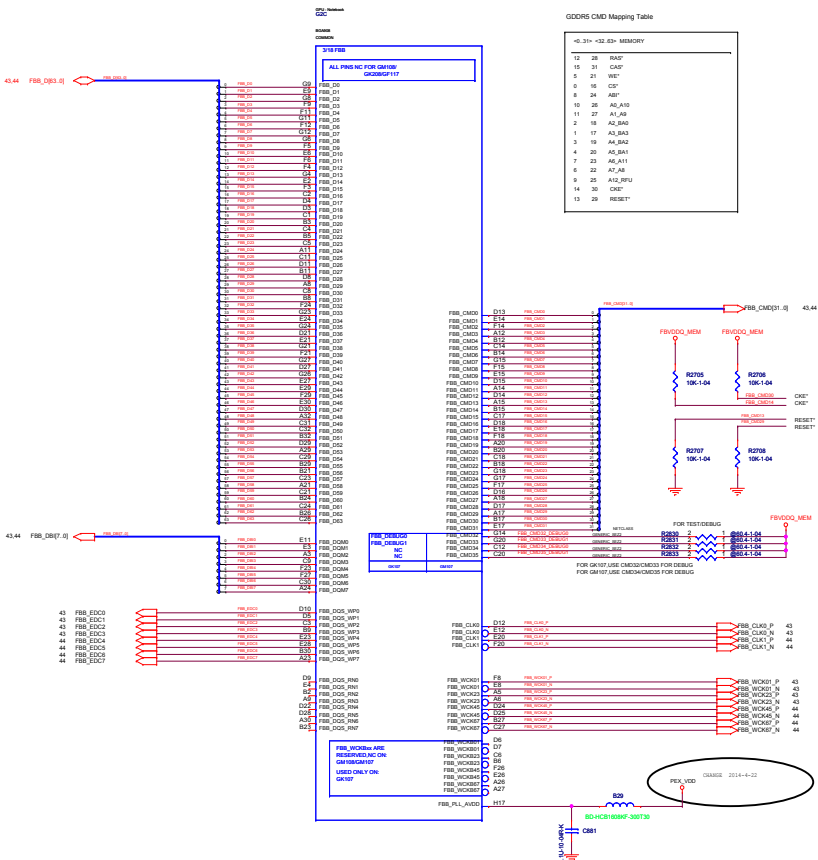
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Size	Document Number
Customer	Customer VCC_PWR 10
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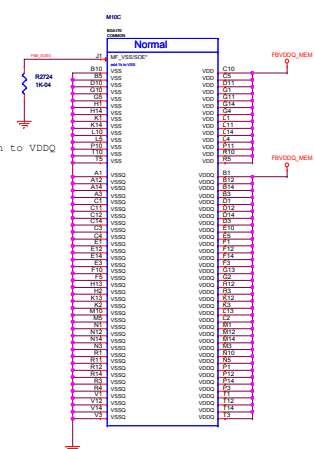
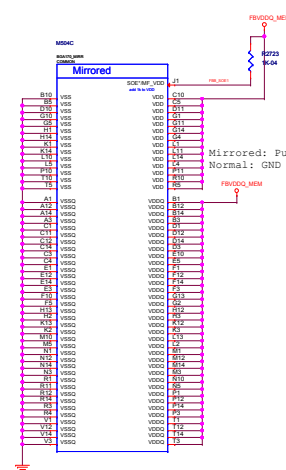
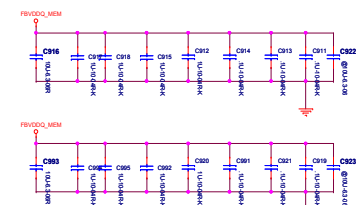
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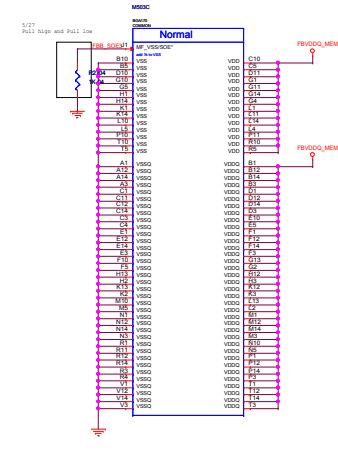
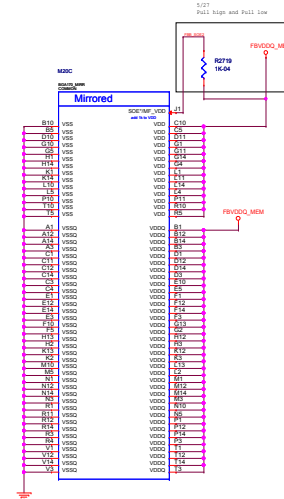
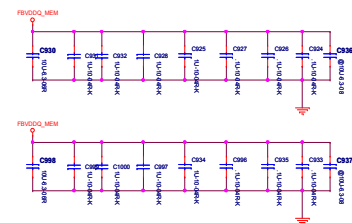
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B	INTEL LAN(82579LM)		RB
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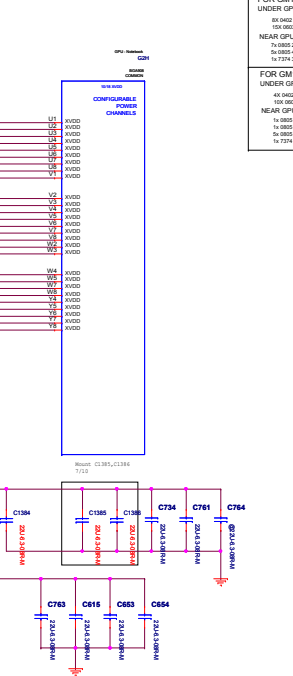
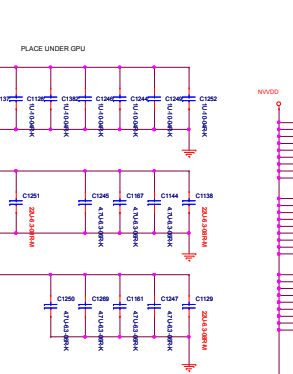
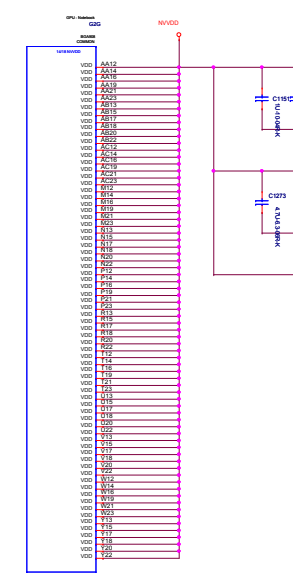
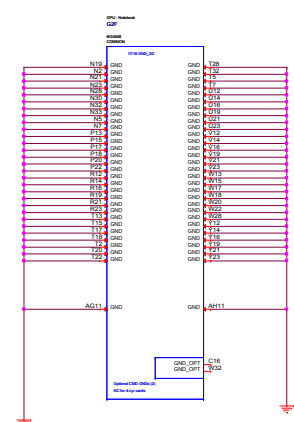
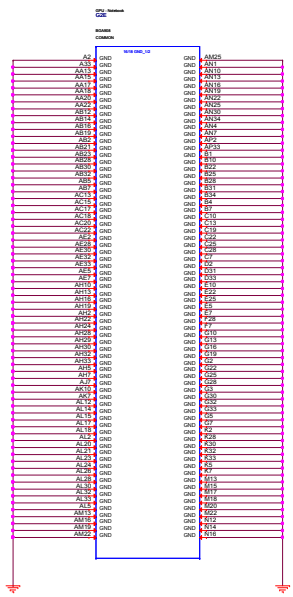
GDPRS CMD Mapping Table

GDPRS CMD Mapping Table	
40-31H ~32-6D- MEMORY	
12	38H BAP
15	31H CASP
5	21H WET
0	16H CS
8	24H ABP
10	26H AL2_A03
11	27H A1_A9
2	18H AL2_A02
1	17H AL2_BA3
3	19H AL2_BA2
4	20H AL2_BA1
7	23H AL2_A11
6	22H AL2_A8
9	25H AL2_RPU
14	30H CRST
13	29H RESET







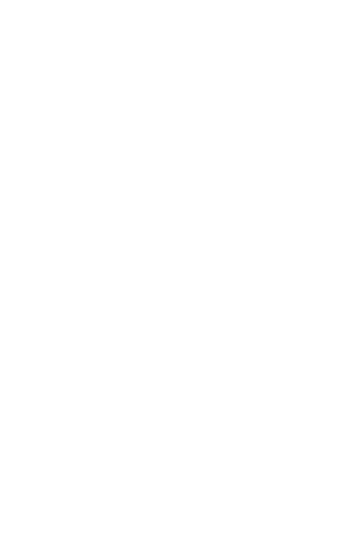
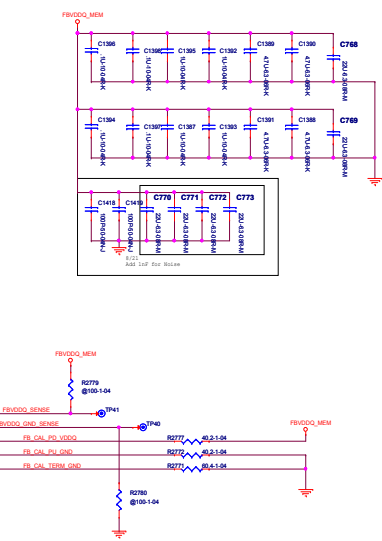
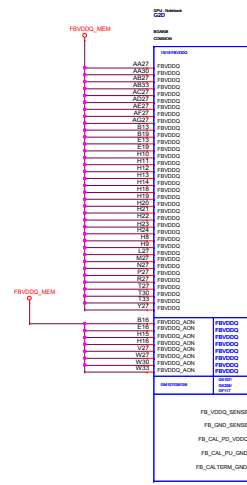


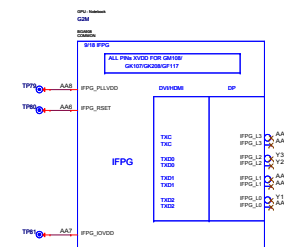
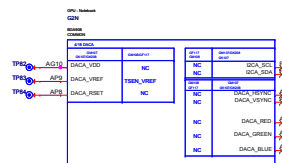
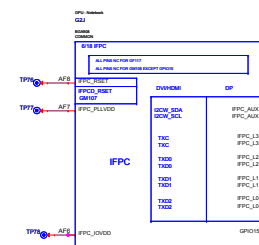
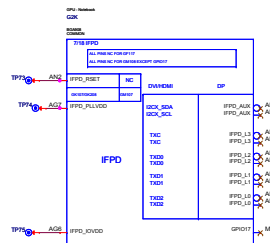
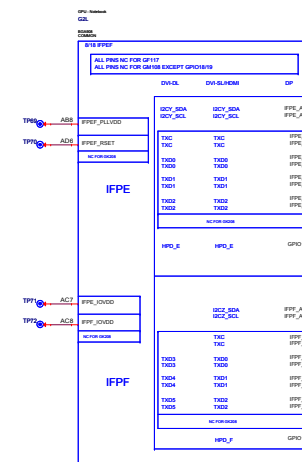
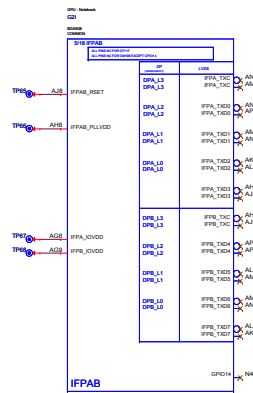
FOR GM107 DECOUPLING CAPS
UNDER GPU

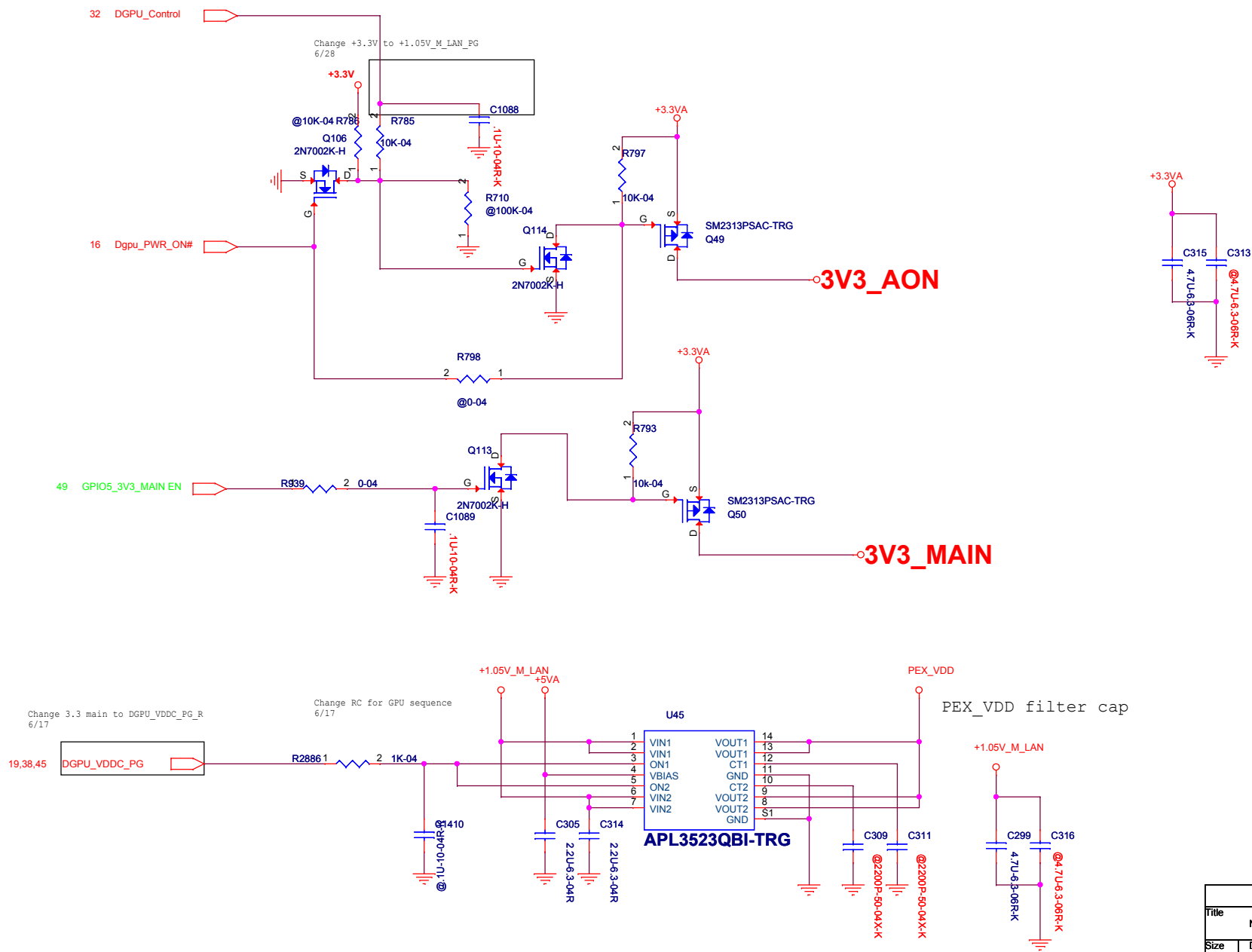
6X 0005 1uF
10X 0005 4.7uF
NEAR GPU
1X 0005 22uF
1X 0005 4.7uF
1X 0005 100uF

FOR GM108 DECOUPLING CAPS
UNDER GPU

6X 0005 1uF
10X 0005 4.7uF
NEAR GPU
1X 0005 22uF
1X 0005 4.7uF
1X 0005 100uF

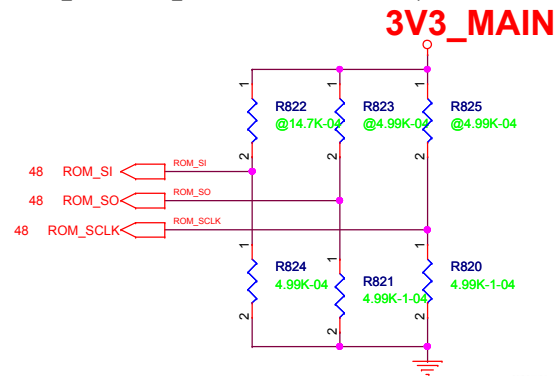






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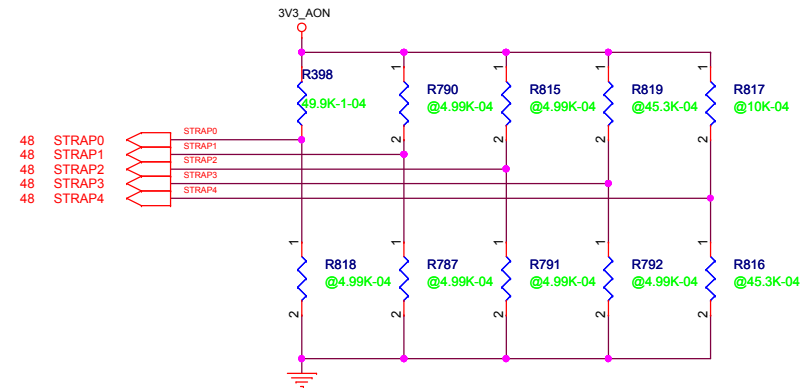
PCI_DEVID5, PCI_DEVID4, & SUBVENDOR Strap Selectable



			R824
Samsung 2G	Samsung 128MX16	0x0	4.99kohm PULL DOWN
HYnix 2G	HYNIX 128MX16	0x1	0kohm PULL DOWN
Micron 2G	MICRON 128MX16	0x5	30.1kohm PULL DOWN
Hynix 4G	HYNIX 256MX16	0x2	15kohm PULL DOWN
Samsung 4G	Samsung 256MX16	0x3	20kohm PULL DOWN
Micron 4G	MICRON 256MX16	0x4	24.9kohm PULL DOWN

Table 11. N15P-GX/GT GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V	128Mx16	Samsung	K4G20325FD-FC03	D-die	0x0	2500	N/A	Production ready
			Hynix	H5GC2H24BFR-T2C	B-die	0x1	2500	1347	Production ready
			Micron	EDW2032BBBG-6A-F	B-die	0x5	2500	N/A	Production ready
		256Mx16	Hynix	H5GC4H24MFR-T2C	A-die	0x2	2500	N/A	Production ready
			Samsung	K4G41325FC-FC03	C-die	0x3	2500	N/A	Production ready
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready



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Data	Change Content	
5.23	CRT power shares with HDMI power for safety requirement	
5.26	NV requirement 1. Delete GC6_FB_EC. 2.EC send adapter in to GPU	
5.27	NV requirement 1. Delete R706 for removal of GC6_EVENT_EC from EC\ Pin 86. 2. Change Pull high and Pull low for VRAM to match mirror VRAM 3. Mount R333	
5.28	Change KB LED TP LED Side LED supply voltage to 5VS Change R659 to 0 OHM	
5.29	1. Change Value to match footprint C358,C936,937,C419, C1001, C1002,C1376 2. Change R824 to 15K	
6.10	Change R344 to 10 mOHM ,NL_R555,NL_B12,Change R842 to 22K, Mount R13,R508,Change R154 to 20K	
6.12	1.Change R228 to 2.43K, Change R233 to 1.5K, NL C274 for Vcore Power Test issue	
6.17	Change GC6 control GPIO connection and GPU power sequence controlled by GPU_Vcore_PG Change C1309 to 1nF	
6.20	Mount R140, NL R141 for eDP detection	
6.21	Page 6: Mount 6Rs Page11: Mount eDP components and remove RT2136 and add a R for PWM Page 16: Mount R481 Page 24 :R140,R141 Page35: NL Side LED	
6.22	1. Add BAT I schematic ,and delete BAT I Direction	
6.27	1. Reserve PG control circuit (mount D21, NL R396) 2. Add EMB dual MOS as 2nd source needing to match OCP resistor	
6.28	1.Change +3.3V to 1.05V_LAN_M_PG(1.Add C1088 2.mount R926 1K C1365) 2. NL R456	
6.30	1. Change R233,R228 C274 for CPU core 2.Add text for Imon explanation	
7.3	1. Add 0 OHM for adjust +1.35, 1.05V 2. Add Boost fan 3. Add 0 OHM for PSI 4. Add 0.1UF*5pcs for EMI 5. Change CPU R228,R233,C274,C285 for TAT 6. NL C243, R555,C1309 7.NL Common choke*1pcs ,Mount 0 OHM *4pcs 8. DMIC : 2pcs resistor, 9. EC control DGPU_ON timing 10. Mount 6pcs cap to CPU Core 11. Add cap to GPU core and VRAM power	
7.4	1.Change U2\vin to 5VA 2. Remove D15 in BAT_I detect circuit 3. Delete Vin AMP,H12 4.Add 0603 CAP to Vcore 5.Reserve POScap to GPU Bottom 6.AC3 PIN2,4 CHANGE NET NAME 7.Change U2 to AZV331	
7.5	1. Mount R27, R28 for mSATA 2. Remove L7 for no Fingerprint 3. Add +3.3Vs on USB board IO for fingerprint 4.Change R337,R319 R value,C274,C258 C value	
7.7	1. Page 6: Add colay R*4 for decreasing eDP signal stub 2. Page 34: correct CN9's SW_BAT pin 3.Add C3209 4.Add Q48 for battery Leakage 5.Update KB pin definition	
7.9	Update Text for VRAM ID R	

